



High Performance, Triple-Output, Auto-Tracking Combo Controller

■ FEATURES

- Provide Triple Accurate Regulated Voltages
- Optimized Voltage-Mode PWM Control
- Dual N-Channel MOSFET Synchronous Drivers
- Fast Transient Response
- Adjustable Over Current Protection using $R_{DS(ON)}$. No External Current Sense Resistor Required.
- Programmable Soft-start Function
- 200KHz Free-Running Oscillator
- Robust Outputs Auto-Tracking Characteristics
- Sink and Source Capabilities with External Circuit

■ APPLICATIONS

- Advanced PC Motherboards
- Information PCs
- Servers and Workstations
- Internet Appliances
- LCD Monitor
- PC add-on Cards
- DDR Termination

■ DESCRIPTION

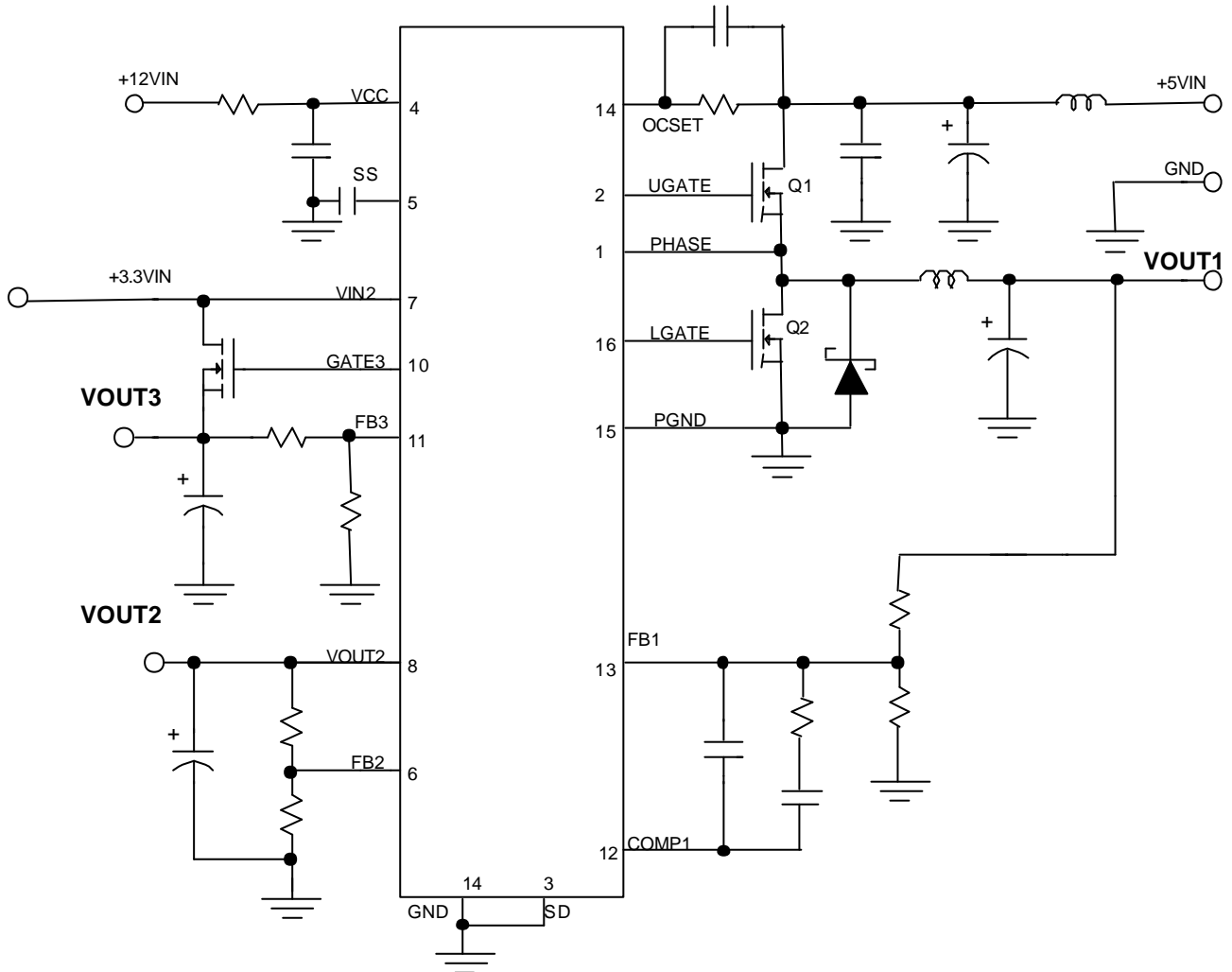
The AIC1340 combines a synchronous voltage mode PWM controller with a low dropout linear regulator and a linear controller as well as the monitoring and protection functions in this chip. The PWM controller regulates the output voltage with a synchronous rectified step-down converter. The built-in N-Channel MOSFET drivers also help to simplify the design of step-down converter. It is able to power CPUs, GPUs, memories, and chipsets. The PWM controller features over current protection using $R_{DS(ON)}$. It improves efficiency and saves cost, as there is no expensive current sense resistor required.

The built-in adjustable linear controller drives an external MOSFET to form a linear regulator that regulates power for system I/O. The built-in adjustable low dropout linear regulator can supply current up to 500mA for supplying another system I/O. Output voltage of both linear regulators can also be adjusted by means of the external resistor divider. Both linear regulators feature current limit. With higher load current required from the low dropout linear regulator, the AIC1341 is recommended.

The programmable soft-start design provides a controlled output voltage rise, which limits the current rate during power on time.

The Shutdown function is also provided for disable the combo controller.

■ TYPICAL APPLICATION CIRCUIT



Typical Triple-Output Application

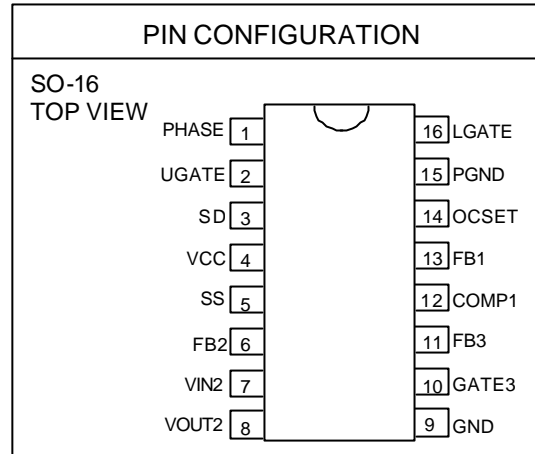
ORDERING INFORMATION

AIC1340CXXX

└─ PACKING TYPE
 TR: TAPE & REEL
 TB: TUBE

 └─ PACKAGING TYPE
 S: SMALL OUTLINE

Example: AIC1340CSTR
 → in SO-16 Package &
 Taping & Reel Packing Type



ABSOLUTE MAXIMUM RATING

Absolute Maximum Ratings

Supply Voltage (VCC) 15V
 UGATE GND - 0.3V to VCC + 0.3V
 LGATE GND - 0.3V to VCC + 0.3V
 Input Output and I/O Voltage GND - 0.3V to 7V

Recommended Operating Conditions

Ambient Temperature Range 0° C to 85° C
 Maximum Operating Junction Temperature 100° C
 Supply Voltage, VCC 15V±10%

Thermal Information

Thermal Resistance θ_{JA} (°C/W)
 SOIC Package 100°C/W
 Maximum Junction Temperature (Plastic Package) 150° C
 Maximum Storage Temperature Range -65° C to 150° C
 Maximum Lead Temperature (Soldering 10s) 300° C

TEST CIRCUIT

Refer to TYPICAL APPLICATION CIRCUIT.

ELECTRICAL CHARACTERISTICS ($V_{cc}=12V$, $T_j=25^\circ C$, Unless otherwise specified)

PARAMETER	TEST CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
VCC SUPPLY CURRENT						
Supply Current	UGATE, LGATE, GATE3 and VOUT2 open	I_{CC}		1.8	3	mA
POWER ON RESET						
Rising VCC Threshold	$V_{OCSET}=4.5V$	$V_{CC_{THR}}$	8.6	9.5	10.4	V
Falling VCC Threshold	$V_{OCSET}=4.5V$	$V_{CC_{THF}}$	8.2	9.2	10.2	V
Rising VIN2 Under-Voltage Threshold		$V_{IN2_{THR}}$	2.5	2.6	2.7	V
VIN2 Under-Voltage Hysteresis		$V_{IN2_{HYS}}$		130		mV
Rising V_{OCSET1} Threshold		V_{OCSETH}		1.3		V
OSCILLATOR and REFERENCE						
Free Running Frequency		F	170	200	230	KHz
FB1 Reference Voltage		V_{REF1}	1.287	1.300	1.313	V
FB2 Reference Voltage		V_{REF2}	1.240	1.265	1.290	V
FB3 Reference Voltage		V_{REF3}	1.250	1.275	1.300	V
LINEAR REGULATOR						
Regulation	$10mA < I_{OUT2} < 150mA$		-1		+1	%
Under-Voltage Level	FB2 falling	$FB2_{UV}$		70	82	%
Over-Current Protection			430	570		mA
Over-Current Protection During Start-up				750		mA
LINEAR CONTROLLER						
Regulation	$0 < I_{GATE3} < 10mA$		-2.5		+2.5	%
Under-Voltage Level	FB3 falling	$FB3_{UV}$		70	80	%

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	TEST CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
PWM CONTROLLER ERROR AMPLIFIER						
DC GAIN				76		dB
Gain Bandwidth Product		GBWP		11		MHz
Slew Rate	COMP1=10pF	SR		6		V/ μ S
PWM CONTROLLER GATE DRIVER						
Upper Drive Source	VCC=12V, V _{UGATE} =11V	R _{UGH}		5.2	6.5	Ω
Upper Drive Sink	VCC=12V, V _{UGATE} =1V	R _{UGL}		3.3	5	Ω
Lower Drive Source	VCC=12V, V _{LGATE} =11V	R _{LGH}		4.1	6	Ω
Lower Drive Sink	VCC=12V, V _{LGATE} =1V	R _{LGL}		3	5	Ω
PROTECTION						
OCSET Current Source	V _{OCSET} =4.5V _{DC}	I _{OCSET}	170	200	230	μ A
Soft-Start Current		I _{SS}		11		μ A
Chip Shutdown Soft Start Threshold					1.0	V

TYPICAL PERFORMANCE CHARACTERISTICS

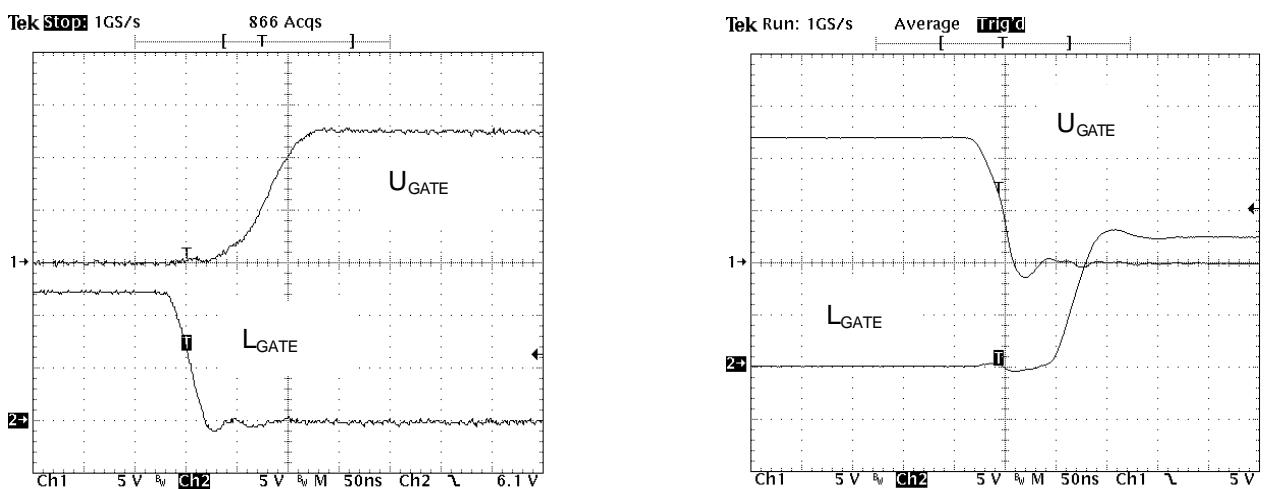


FIG.1 The gate drive waveforms

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

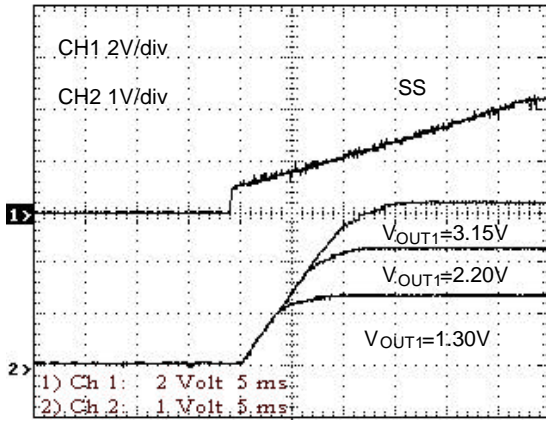


FIG. 2 Soft Start Initiates PWM Output

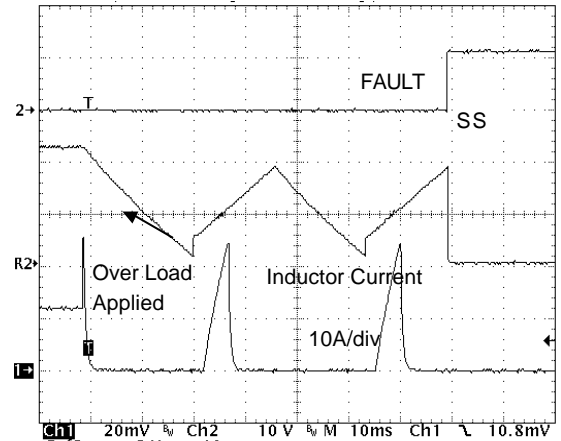


FIG. 3 Over-Current Operation on Inductor

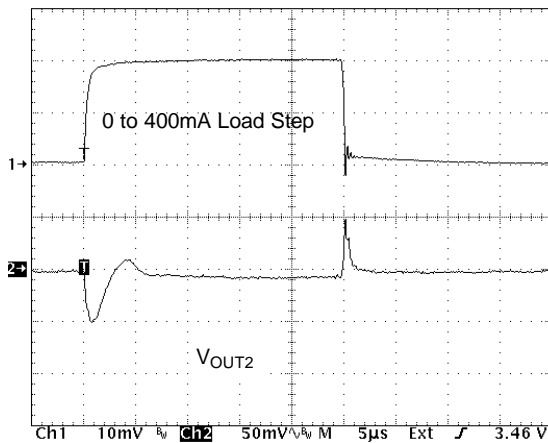


FIG. 4 Transient Response of Linear Regulator

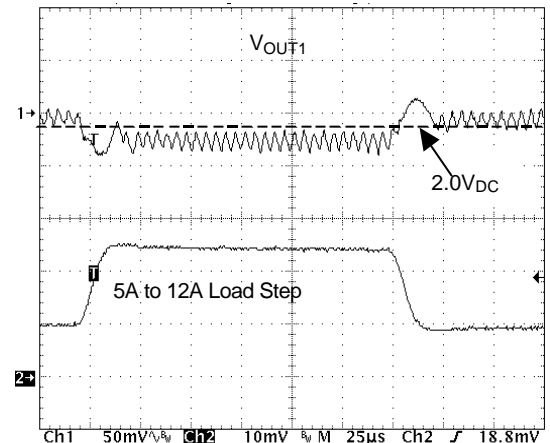


FIG. 5 Transient Response of PWM Output

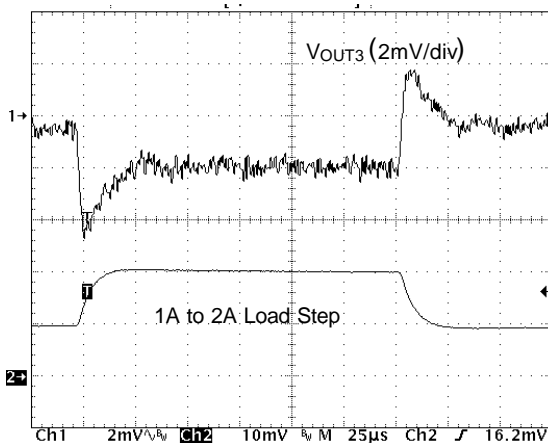


FIG. 6 Transient Response of Linear Controller

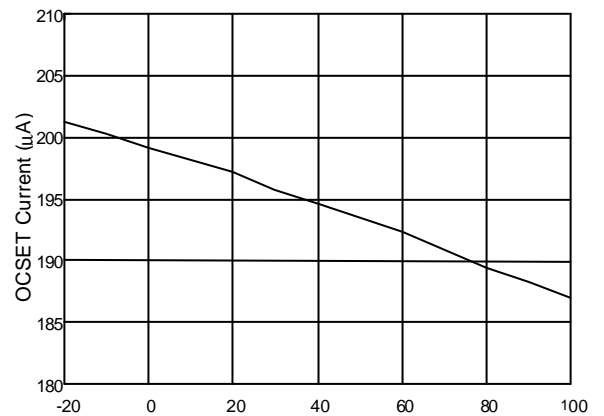


FIG. 7 OCSET Current vs. Temperature (°C)

■ **TYPICAL PERFORMANCE CHARACTERISTICS (Continued)**

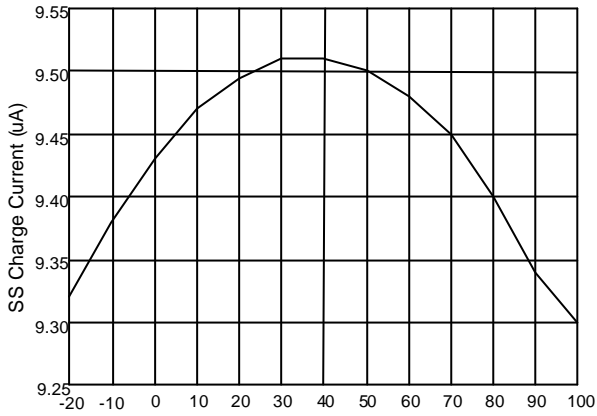


FIG.8 SS Current vs. Temperature (°C)

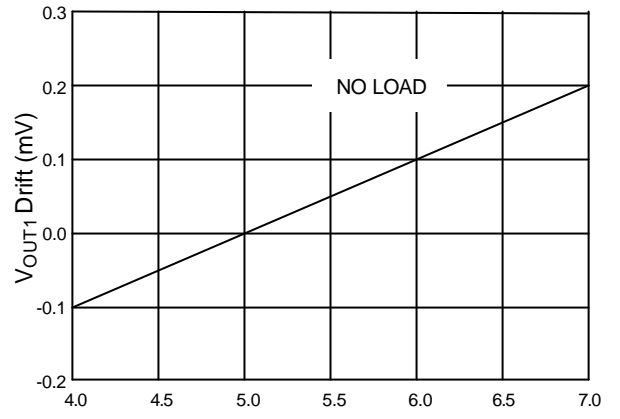
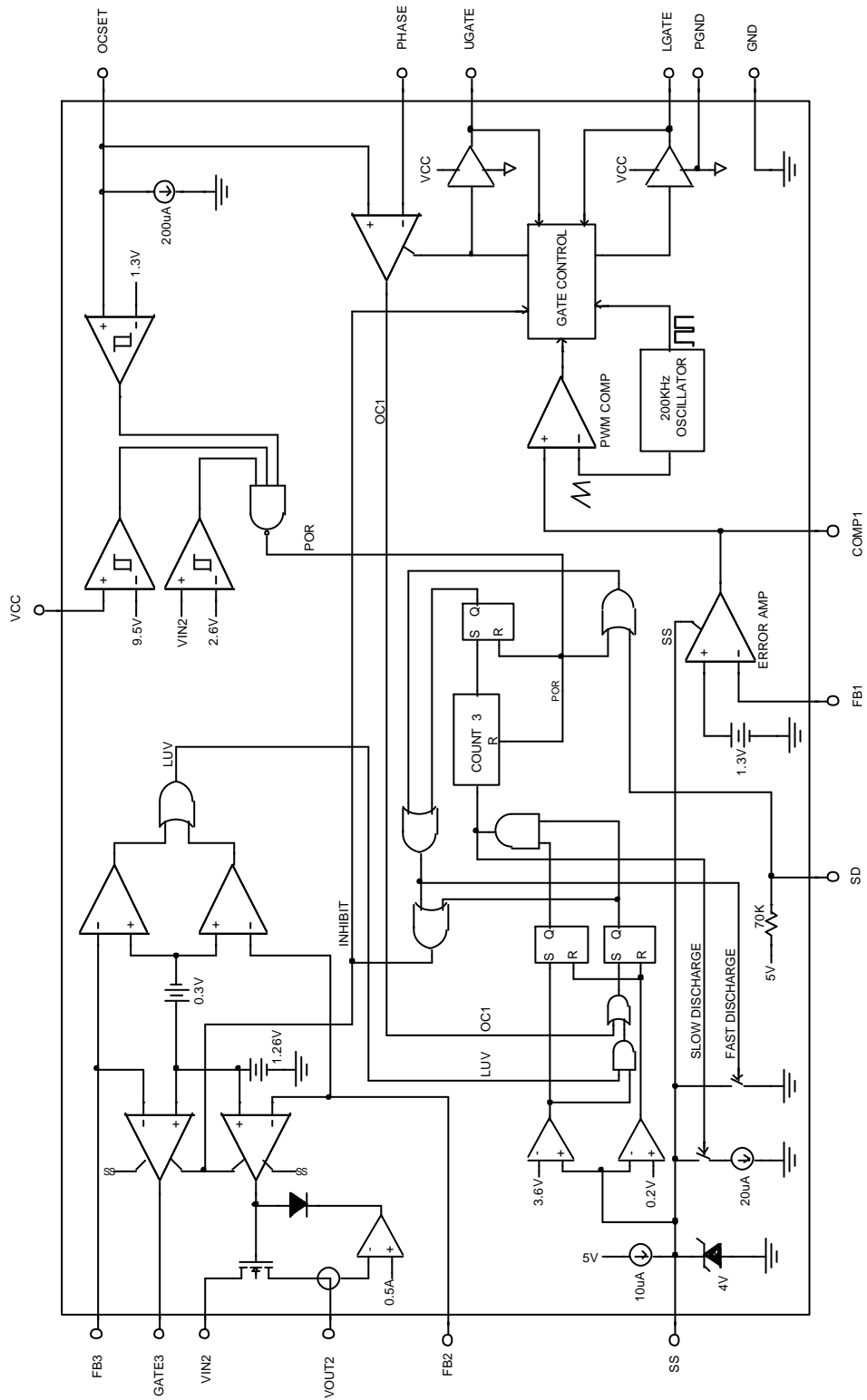


FIG.9 V_{OUT1} Drift vs. VIN (V)

■ BLOCK DIAGRAM



■ PIN DESCRIPTIONS

- Pin 1: PHASE: Over-current detection pin. Connect the PHASE pin to source of the external high-side N-MOSFET. This pin detects the voltage drop across the high-side N-MOSFET RDS(ON) for over-current protection. Additionally, this pin is used to monitor the 3.3V supply. If, following a start-up cycle, the voltage drops below 2.6V (typically), the chip shuts down. A new soft-start cycle is initiated upon return of the 3.3V supply above the under-voltage threshold.
- Pin 2: UGATE: External high-side N-MOSFET gate drive pin. Connect UGATE to gate of the external high-side N-MOSFET.
- Pin 3: SD: To shut down the system, active high or floating. Keep the resistor less than 4.7K Ω if a resistor attached to ground.
- Pin 4: VCC: The chip power supply pin. It also provides the gate bias charge for all the MOSFETs controlled by the IC. Recommended supply voltage is 12V.
- Pin 5: SS: Soft-start pin. Connect a capacitor from this pin to ground. This capacitor, along with an internal 10 μ A (typically) current source, sets the soft-start interval of the converter. Pulling this pin low will shut down the IC.
- Pin 6: FB2: Connect this pin to a resistor divider to set the linear regulator output voltage.
- Pin 7: VIN2: This pin supplies power to the internal regulator. Connect this pin to a suitable 3.3V source.
- Pin 8: VOUT2: Output of the linear regulator. Supplies current up to 500mA.
- Pin 9: GND: Signal GND for IC. All voltage levels are measured with respect to this pin. Keep the trace close to the ground side of the output capacitor.
- Pin 10: GATE3: Linear Controller output drive pin. This pin can drive either a Darlington NPN transistor or a N-channel MOSFET.
- Pin 11: FB3 Negative feedback pin for the linear controller error amplifier connect this pin to a resistor divider to set the linear controller output voltage.
- Pin 12: COMP1 External compensation pin. This pin is connected to error amplifier output and PWM comparator. An RC network is connected to FB1 in to compensate the voltage control feedback loop of the converter.
- Pin 13: FB1 The error amplifier inverting input pin. the FB1 pin and COMP1 pin are used to

compensate the voltage-control feedback loop.

Pin 14: OCSET: Current limit sense pin. Connect a resistor R_{OCSET} from this pin to the drain of the external high-side N-MOSFET. R_{OCSET} , an internal $200\mu A$ current source (I_{OCSET}), and the upper N-MOSFET on-resistance ($R_{DS(ON)}$) set the over-current trip point according to the following equation:

$$I_{PEAK} = \frac{I_{OCSET} \times R_{OCSET}}{R_{DS(ON)}}$$

Pin 15: PGND: Driver power GND pin. PGND should be connected to a low impedance ground plane in close to lower N-MOSFET source.

Pin 16: LGATE: Lower N-MOSFET gate drive pin.

■ APPLICATIONS INFORMATION

The AIC1340 is designed for multiple power applications. This IC has one PWM controller, a linear regulator, and a linear controller. The PWM controller is designed to regulate the voltage (V_{OUT1}) by driving 2 MOSFETs (Q1 and Q2) in a synchronous rectified buck converter configuration. The voltage is regulated to a level programmed by the resistive network composed of 2 resistors. An integrated linear regulator supplies the regulated DC source (V_{OUT2}) with the 500mA driving current. The linear controller drives an external MOSFET(Q3) to supply the DC power (V_{OUT3}).

The Power-On Reset (POR) function continually monitors the input supply voltage at VCC pin, OCSET pin, and VIN2 pin. The POR function initiates soft-start operation after all three input supply voltage exceed their POR thresholds.

Soft-Start

The POR function initiates the soft-start sequence. Initially, the voltage on SS pin rapidly increases to approximate 1V. Then an internal $10\mu A$ current

source charges an external capacitor (C_{SS}) on the SS pin to 4V. As the SS pin voltage slews from 1V to 4V, the PWM error amplifier reference input (Non-inverting terminal) and output (COMP1 pin) is clamped to a level proportional to the SS pin voltage. As the SS pin voltage slew from 1V to 4V, the output clamp generates PHASE pulses of increasing width that charge the output capacitors. Additionally both linear regulators' reference inputs are clamped to a voltage proportional to the SS pin voltage. This method provides a controlled output voltage smooth rise.

Fig.2 shows the soft-start sequence for the typical application. The internal oscillator's triangular waveform is compared to the clamped error amplifier output voltage. As the SS pin voltage increases, the pulse width on PHASE pin increases. The interval of increasing pulse width continues until output reaches sufficient voltage to transfer control to the input reference clamp.

Each linear output (V_{OUT2} and V_{OUT3}) initially follows a ramp. When each output reaches

sufficient voltage the input reference clamp slows the rate of output voltage rise.

Over-Current Protection

All outputs are protected against excessive over-current. The PWM controller uses upper MOSFET's on-resistance, $R_{DS(ON)}$ to monitor the current for protection against shorted outputs. The linear regulator monitors the current limit in excess of 500mA. Additionally, both the linear regulator and controller monitor FB2 and FB3 for under-voltage to protect against excessive current.

When the voltage across Q1 ($I_D \times R_{DS(ON)}$) exceeds the level ($200\mu A \times R_{OCSET}$), this signal inhibit all outputs. Discharge soft-start capacitor (C_{SS}) with $10\mu A$ current sink, and increments the counter. C_{SS} recharges and initiates a soft-start cycle again until the counter increments to 3. This sets the fault latch to disable all outputs. Fig. 3 illustrates the over-current protection until an over load on OUT1.

Should excessive current cause FB2 or FB3 to fall below the linear under-voltage threshold, the LUV signal sets the over-current latch if C_{SS} is fully charged. Cycling the bias input power off then on reset the counter and the fault latch.

The over-current function for PWM controller will trip at a peak inductor current (I_{PEAK}) determined by:

$$I_{PEAK} = \frac{I_{OCSET} \times R_{OCSET}}{R_{DS(ON)}}$$

The OC trip point varies with MOSFET's temperature. To avoid over-current tripping in the normal operating load range, determine the R_{OCSET} resistor from the equation above with:

1. The maximum $R_{DS(ON)}$ at the highest junction.
2. The minimum I_{OCSET} from the specification table.
3. Determine:

$$I_{PEAK} > I_{OUT(MAX)} + \frac{\text{Inductor Ripple Current}}{2}$$

Shutdown

Holding the SD pin high to turn off all three regulators. If a resistor attached to ground, keep the resistor less than $4.7K\Omega$.

Layout Considerations

Any inductance in the switched current path generates a large voltage spike during the switching interval. The voltage spikes can degrade efficiency, radiate noise into the circuit, and lead to device over-voltage stress. Careful component selection and tight layout of critical components, and short, wide metal trace minimize the voltage spike.

- 1) A ground plane should be used. Locate the input capacitors (C_{IN}) close to the power switches. Minimize the loop formed by C_{IN} , the upper MOSFET (Q1) and the lower MOSFET (Q2) as possible. Connections should be as wide as short as possible to minimize loop inductance.
- 2) The connection between Q1, Q2 and output inductor should be as wide as short as practical. Since this connection has fast voltage transitions will easily induce EMI.
- 3) The output capacitor (C_{OUT}) should be located as close the load as possible. Because minimize the transient load magnitude for high slew rate requires low inductance and resistance in circuit board

4) The AIC1340 is best placed over a quiet ground plane area. The GND pin should be connected to the groundside of the output capacitors. Under no circumstances should GND be returned to a ground inside the C_{IN} , Q1, Q2 loop. The GND and PGND pins should be shorted right at the IC. This help to minimize internal ground disturbances in the IC and prevents differences in ground potential from disrupting internal circuit

operation.

- 5) The wiring traces from the control IC to the MOSFET gate and source should be sized to carry 1A current. The traces for OUT2 need only be sized for 0.5A. Locate C_{OUT2} close to the AIC1340 IC.
- 6) The V_{CC} pin should be decoupled directly to GND by a 1uF ceramic capacitor, trace lengths should be as short as possible.

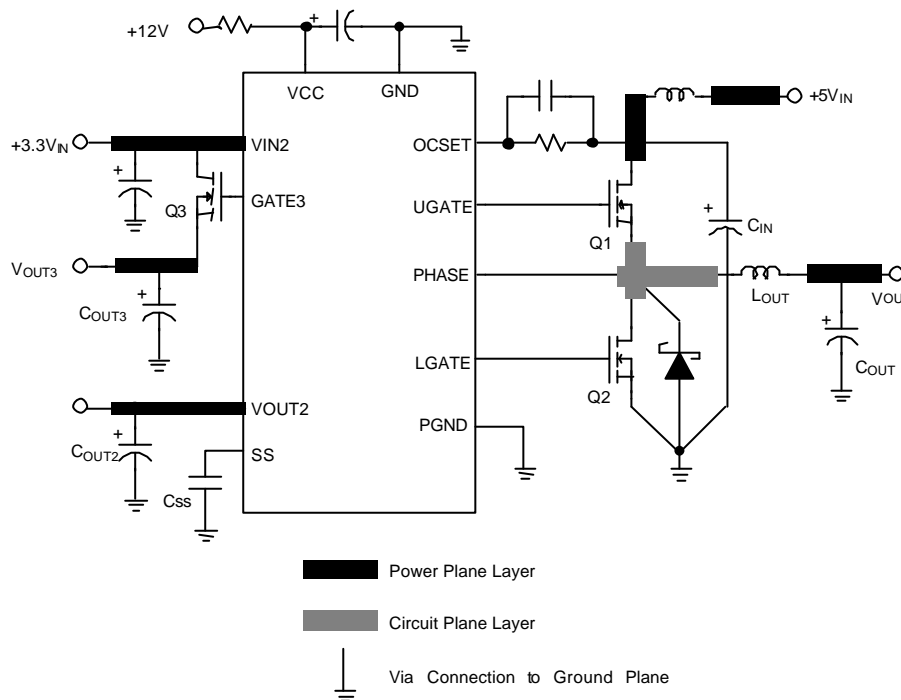


Fig. 10 Printed circuit board power planes and islands

A multi-layer-printed circuit board is recommended. Figure 10 shows the connections of the critical components in the converter. The C_{IN} and C_{OUT} could each represent numerous physical capacitors. Dedicate one solid layer for a ground plane and make all critical component

ground connections with vias to this layer.

PWM Output Capacitors

The load transient for the some applications such as microprocessor core requires high quality capacitors to supply the high slew rate (di/dt) current demand.

The ESR (equivalent series resistance) and ESL (equivalent series inductance) parameters rather than actual capacitance determine the buck capacitor values. For a given transient load magnitude, the output voltage transient change due to the output capacitor can be noted by the following equation:

$$\Delta V_{OUT} = ESR \times \Delta I_{OUT} + ESL \times \frac{\Delta I_{OUT}}{\Delta T}, \quad \text{where}$$

ΔI_{OUT} is transient load current step.

After the initial transient, the ESL dependent term drops off. Because the strong relationship between output capacitor ESR and output load transient, the output capacitor is usually chosen for ESR, not for capacitance value. A capacitor with suitable ESR will usually have a larger capacitance value than is needed for energy storage.

A common way to lower ESR and raise ripple current capability is to parallel several capacitors. In most cases, multiple electrolytic capacitors of small case size are better than a single large case capacitor.

Output Inductor Selection

Inductor value and type should be chosen based on output slew rate requirement, output ripple requirement and expected peak current. Inductor value is primarily controlled by the required current response time. The AIC1340 will provide either 0% or 100% duty cycle in response to a load transient. The response time to a transient is different for the application of load and remove of load.

$$t_{RISE} = \frac{L \times \Delta I_{OUT}}{V_{IN} - V_{OUT}},$$

$t_{FALL} = \frac{L \times \Delta I_{OUT}}{V_{OUT}}$. Where ΔI_{OUT} is transient load current step.

In a typical 5V input, 2V output application, a 3 μ H inductor has a 1A/ μ S rise time, resulting in a 5 μ S delay in responding to a 5A load current step. To optimize performance, different combinations of input and output voltage and expected loads may require different inductor values. A smaller value of inductor will improve the transient response at the expense of increased output ripple voltage and inductor core saturation rating.

Peak current in the inductor will be equal to the maximum output load current plus half of inductor ripple current. The ripple current is approximately equal to:

$$I_{RIPPLE} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{f \times L \times V_{IN}};$$

$f = 200\text{KHz}$ in AIC1340 application.

The inductor must be able to withstand peak current without saturation, and the copper resistance in the winding should be kept as low as possible to minimize resistive power loss.

Input Capacitor Selection

Most of the input supply current is supplied by the input bypass capacitor, the resulting RMS current flow in the input capacitor will heat it up. Use a mix of input bulk capacitors to control the voltage overshoot across the upper MOSFET. The ceramic capacitance for the high frequency decoupling should be placed very close to the upper MOSFET to suppress the voltage induced in the parasitic circuit impedance. The buck capacitors to supply the RMS current is approximately equal to:

$$I_{RMS} = (1-D) \times \sqrt{D} \times \sqrt{I_{OUT}^2 + \frac{1}{12} \times \left(\frac{V_{IN} \times D}{f \times L} \right)^2}$$

, where $D = \frac{V_{OUT}}{V_{IN}}$

The capacitor voltage rating should be at least 1.25 times greater than the maximum input voltage.

PWM MOSFET Selection

In high current PWM application, the MOSFET power dissipation, package type and heatsink are the dominant design factors. The conduction loss is the only component of power dissipation for the lower MOSFET, since it turns on into near zero voltage. The upper MOSFET has conduction loss and switching loss. The gate charge losses are proportional to the switching frequency and are dissipated by the AIC1340. However, the gate charge increases the switching interval, t_{SW} which increase the upper MOSFET switching losses. Ensure that both MOSFETs are within their maximum junction temperature at high ambient temperature by calculating the temperature rise according to package thermal resistance specifications.

$$P_{UPPER} = I_{OUT}^2 \times R_{DS(ON)} \times D + \frac{I_{OUT} \times V_{IN} \times t_{SW} \times f}{2}$$

$$P_{LOWER} = I_{OUT}^2 \times R_{DS(ON)} \times (1-D)$$

The equations above do not model power loss due to the reverse recovery of the lower MOSFET's body diode.

The $R_{DS(ON)}$ is different for the two previous equations even if the type devices is used for

both. This is because the gate drive applied to the upper MOSFET is different than the lower MOSFET. Logic level MOSFETs should be selected based on on-resistance considerations, $R_{DS(ON)}$ should be chosen base on input and output voltage, allowable power dissipation and maximum required output current. Power dissipation should be calculated based primarily on required efficiency or allowable thermal dissipation.

Rectifier Schottky diode is a clamp that prevent the loss parasitic MOSFET body diode from conducting during the dead time between the turn off of the lower MOSFET and the turn on of the upper MOSFET. The diode's rated reverse breakdown voltage must be greater than twice the maximum input voltage.

Linear Controller MOSFET Selection

The power dissipated in a linear regulator is :

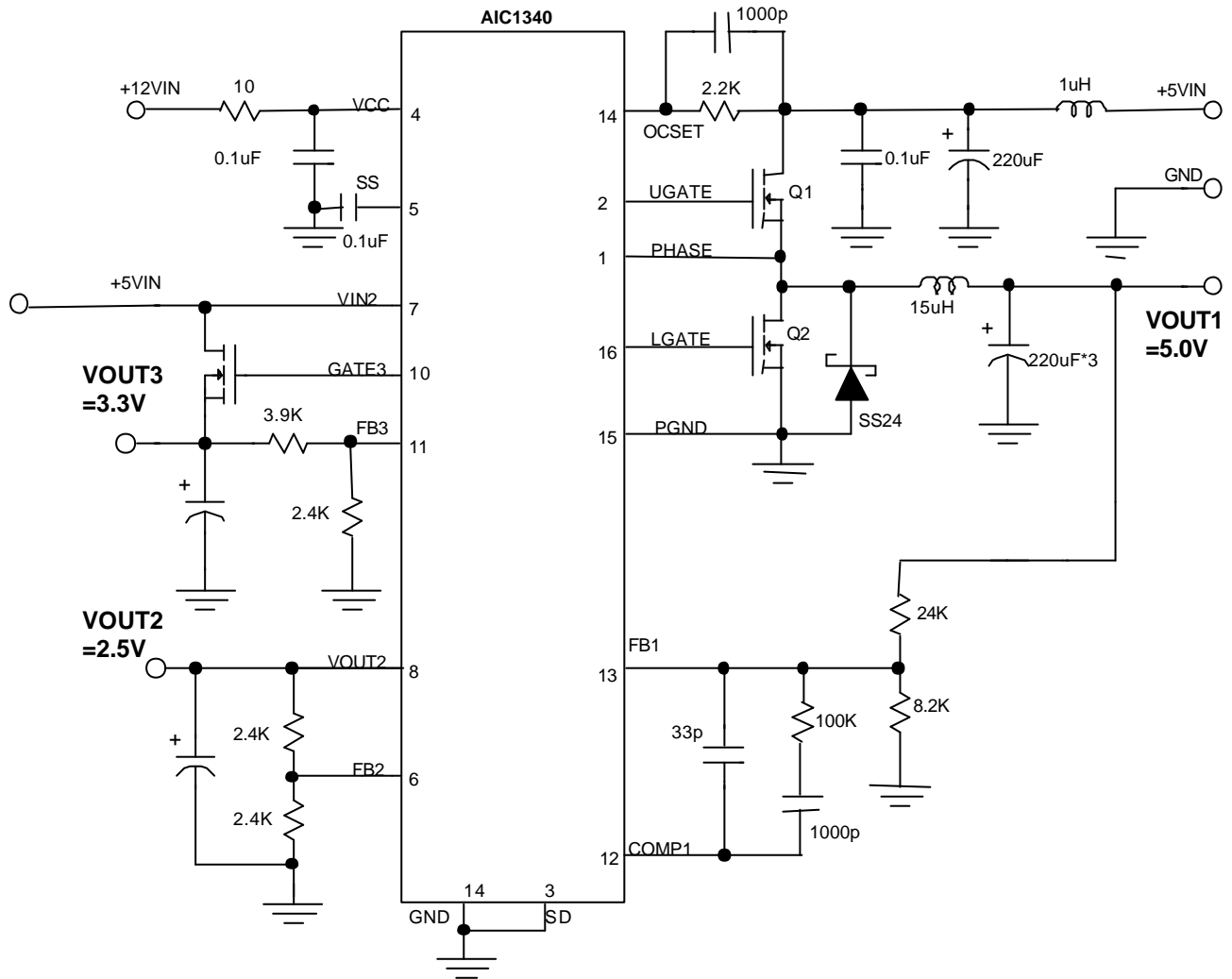
$$P_{LINEAR} = I_{OUT2} \times (V_{IN2} - V_{OUT2})$$

Select a package and heatsink that maintains junction temperature below the maximum rating while operation at the highest expected ambient temperature.

Linear Output Capacitor

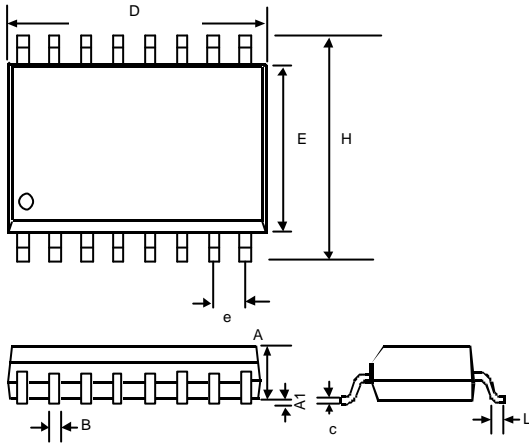
The output capacitors for the linear regulator and linear controller provide dynamic load current. The linear controller uses dominant pole compensation integrated in the error amplifier and is insensitive to output capacitor selection. C_{OUT3} should be selected for transient load regulation. The output capacitor for the linear regulator provides loop stability.

APPLICATION CIRCUIT



■ PHYSICAL DIMENSIONS

- 16 LEAD PLASTIC SO (300 mil) (unit: mm)



SYMBOL	MIN	MAX
A	2.35	2.65
A1	0.10	0.30
B	0.33	0.51
C	0.23	0.32
D	10.10	10.50
E	7.40	7.60
e	1.27(TYP)	
H	10.00	10.65
L	0.40	1.27