

# The effect of ESR on DC/DC power converter

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## Introduction

The capacitors, inductors, and resistors in circuit analysis have ideal properties. Capacitors and inductors follow precise derivative relationships. In the real world, components do not follow such simple models. The non-ideal behavior of energy storage components is very important in the context of power electronics. This article is to discuss the effect of capacitor's ESR (Equivalent series Resistor) characteristics on DC/DC power converter. And now, capacitors shall be presenting first.

## Capacitors- Principles and Equivalent Circuits

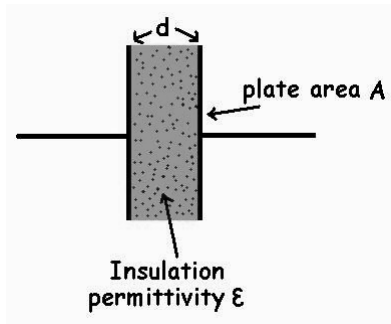


Figure 1. The basic parallel-plate capacitor geometry<sub>[1]</sub>

Capacitor devices come in many forms, but nearly all of them are composed of conducting plates or films, also separated by an insulating layer such as air or paper. A common parallel arrangement, shown in figure 1, gives equation 1 as follows.

$$C = \frac{\epsilon A}{d} \dots\dots\dots(\text{equ.1})$$

where  $\epsilon$  is the electrical permittivity of the insulating layer,  $A$  is the surface area, and  $d$  is the distance between 2 plates. By definition, the magnitude of the charge  $Q$  stored on either plates of the capacitor is directly proportional to the potential difference  $V$  between the plates. Therefore, we may write

$$Q = CV \dots\dots\dots(\text{equ.2})$$

where  $V$  is the applied voltage. In the arrangement of parallel plates, the electric field is given by

$$E = \frac{V}{d} \dots\dots\dots(\text{equ.3})$$

The time derivative of  $Q=CV$  gives the standard property

$$i = C \frac{dv}{dt} \dots\dots\dots(\text{equ.4})$$

The parallel plate arrangement has provided some challenges for years. Picture that two plates with measurements of one square meter for both plates, which are separated by 1um air space, form a capacitor of less than 10µF. Nevertheless, typical capacitors used in power converter are usually on the order of 100µF or more. However, the permittivity of free space or air is small, with  $\epsilon_0 = 8.854\text{pF/m}$  and very large plates are required to give significant values of  $C$ . But the effect of inserting the dielectric is

to increase the capacitance by a factor of dielectric constant k.

$$K = \frac{\epsilon}{\epsilon_0} \dots\dots\dots (\text{equ.5})$$

Typical values of k are shown in table 1 as below.

Table1. Dielectric Constant and Strength

Material	Dielectric Constant	Dielectric Strength(10 <sup>6</sup> V/m)
Air	1.00059	3
Paper	3.7	16
Glass	4~6	9
Paraffin	2.3	11
Rubber	2~3.5	30
Mica	6	150
Water	80	-

Although the term “dielectric” is nearly invariable applied to insulating materials, which is somewhat a misleading. Water, which has a high dielectric constant, is not an insulator.

In a capacitor device, the wires and plates have resistance and inductance. The insulation is not perfect and has a leakage resistance. These direct properties can be summarized in a circuit model, shown in figure 2.[2]

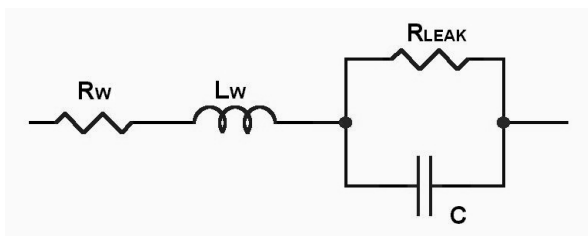


Figure 2. General circuit model for a real capacitor

The properties of the model can be minimized, but not be avoided altogether. This equivalent exhibits numbers of important properties.

- The current is not exactly consistent with  $i=Cdv/dt$
- Current flows even when dc voltage is applied
- Resonance occurred due to the combination of L and C. The device behaves as an inductor when operated at a frequency which is over the resonant frequency.
- Extra power loss

The properties are out of consideration in general applications. However, they play as a decisive role in some of the applications for high operating frequency or low voltage with high current, e.g. VRMx.x.

The inductance is expected to be in the nano-henry (10<sup>-9</sup>H) range, since it represents wire inductance and geometric effect. The leakage resistance should be very high, and the time constant of the insulation,

$$\tau = R_{LEAK}C \dots\dots\dots (\text{equ.6})$$

should be very long.

In many power electronics applications, a capacitor is to be used at a specific frequency. Given a radian frequency  $\omega$ , the circuit model can be evaluated as a set of impedance, then simplified. The simplified one is shown in figure 3, the derivation starts with a capacitor C in parallel with the leakage resistance  $R_{LEAK}$ .

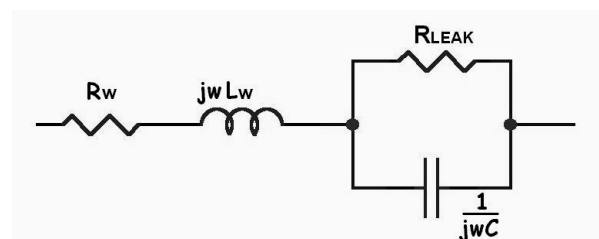


Figure 3.

Fig. 3 can be turned into an equivalent series, as figure 4, after some certain mathematical transform.

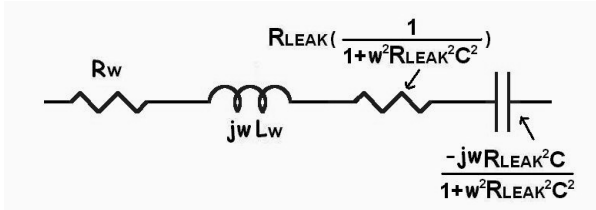


Figure 4.

Since  $R_{LEAK}C$  is high,  $\omega^2 R_{LEAK}^2 C^2 \gg 1$  is true as the frequency goes above about 1Hz. Then the reactance portion simplifies to  $\frac{-j}{\omega C}$ . The series resistance portion simplifies to  $\frac{1}{\omega^2 R_{LEAK} C^2}$ . It gets much “lovelier” for the exhibition in figure 5, comparing with figure 4.

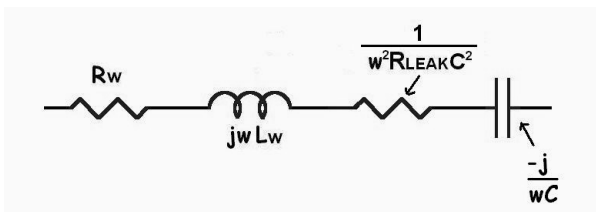


Figure 5.

Till now, the equivalent circuit has been simplified to a series R-L-C combination. The inductor in the circuit is termed as an equivalent series inductance or ESL. The capacitor represents the internal ideal capacitance effect. The resistor, termed as an equivalent series resistance or ESR, has the value of

$$ESR = R_w + \frac{1}{\omega^2 R_{LEAK} C^2} \dots\dots\dots (equ.7)$$

The combination, shown in figure 6, is sometimes called as a standard model of a capacitor. It has been

widely used by manufacturers as the basis of specifications. Since the ESR is obtained through a transformation, therefore, it is a non-linear frequency-dependent resistance. The value is given at a specific frequency (120Hz or 100KHz is common) on data sheets.

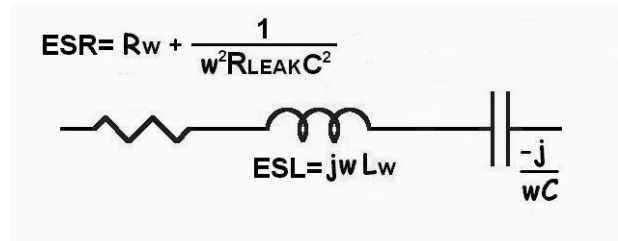


Figure 6. The standard model of a capacitor

Besides, the parameter, dissipation factor  $df$ , is often used to indicate the quality of a capacitor. It shows the ratio of resistance to reactance. For the frequency below  $\frac{1}{\sqrt{ESLC}}$ , the standard model’s reactance is approximately  $\frac{1}{\omega C}$ , which gives

$$df = \frac{R}{X} = (ESR)\omega E \dots\dots\dots (equ.8)$$

The ratio is also called loss tangent,  $df$ , coming with an impedance angle  $\phi = \tan^{-1}(\frac{X}{R})$ . If the wire resistance is small, the ESR becomes the second term in equation 7 and the dissipation factor can be written as

$$df = \tan \delta = ESR\omega C \doteq \frac{\omega C}{\omega^2 R_{LEAK} C^2} = \frac{1}{\omega R_{LEAK} C} \dots\dots (equ.9) \circ$$

The leakage resistance can be calculated from the resistivity of insulation,  $\rho$ , since the geometry is known. We substitute  $\frac{\epsilon A}{d}$  and  $\frac{\rho d}{A}$  for C and  $R_{LEAK}$

and derive the result  $\tan \delta = \frac{1}{\omega \epsilon \rho}$  from equation 9.

Thus the loss tangent is independent of geometry and can be considered a material property associated with the insulator. **That is, the ESR value strongly depends on the choice of insulation material.**

### The effect of ESR

Unfortunately, the effect of ESR will never disappear. Below the resonant frequency, a real capacitor will show a resistance in series with a capacitive reactance. The capacitor becomes a simple RC series combination. In some applications such as a DC/DC converter, a capacitor is often exposed to a square wave of current. Ideally, this produces a triangular voltage across the part shown in figure 7.

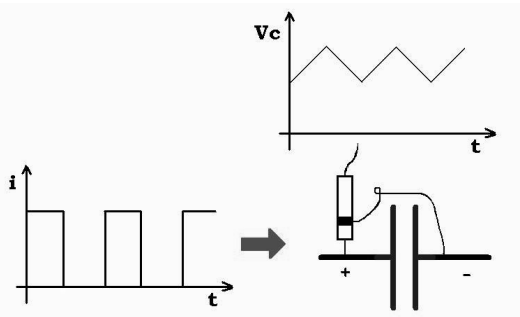


Figure 7.

But to lead to some unusual result, the ESR will exhibit an ESR voltage drop. With the ESR, a small square wave adds in series with the triangle, the abrupt voltage change called an ESR jump. In some case, it can dominate over ripple during the design process. Even when LDO used, the ESR effect

appears as the variation loading current applied.

### Tutorial example

#### Switching mode power supply part

As the IT market grows rapidly, the device power requirement is getting more and more complicated. Obviously, one trend is to use the switching mode power supply instead of conventional linear regulator, which betters the efficiency.

This design example, as shown in figure 8, provides an output voltage of 1.3V to 3.5V, which meets the VRM8.4 specification. It can deliver high current to a CPU  $V_{CORE}$  load. According to the tight VRM transient demand, the effect of ESR plays a significant role in the application.

### **AIC1570- Advanced PWM Switching and Dual Linear Controller IC!!!**

The AIC1570 combines a synchronous voltage mode controller with a low dropout linear regulator and a linear controller as well as the monitoring and protection functions in this chip. The PWM controller regulates the microprocessor core voltage with a synchronous rectified buck converter. The linear controller regulates power for the GTL bus and the linear regulator provides power for the clock driver circuit.

An integrated 5 bit D/A converter that adjusts the core PWM output voltage from 2.1V to 3.5V in 0.1V increments and from 1.3V to 2.05V in 0.05V increments. The linear regulator uses an internal driver device to provide  $2.5V \pm 2.5\%$ . The linear controller drives with an external N-channel MOSEFET to provide  $1.5V \pm 2.5\%$ .

### **Features**

- Provides 3 Regulated Voltages for Microprocessor Core, Clock and GTL Power.
- Simple Voltage-Mode PWM Control.
- Dual N-Channel MOSFET Synchronous Driver.
- Operates from +3.3V, +5V and +12V Inputs
- Fast Transient Response.
- Full 0% to 100% Duty Ratios.
- $\pm 1.0\%$  Output Voltage for  $V_{CORE}$  and  $\pm 2.0\%$  Output Voltage Reference for  $V_{CLK}$  and  $V_{GTL}$ .
- TTL Compatible 5-bit Digital-to-Analog Core Output Voltage Selection. Range from 1.3V to 3.5V.
- 0.1V Steps from 2.1V to 3.5V., 0.05V Steps from 1.3V to 2.05V.
- Adjustable Current Limit without External Sense Resistor.
- Microprocessor Core Voltage Protection against Shorted MOSFET.
- Power Good Output Voltage Monitor.
- Over-Voltage and Over-Current Fault Monitors.
- 200KHz Free-Running Oscillator Programmable up to 350KHz

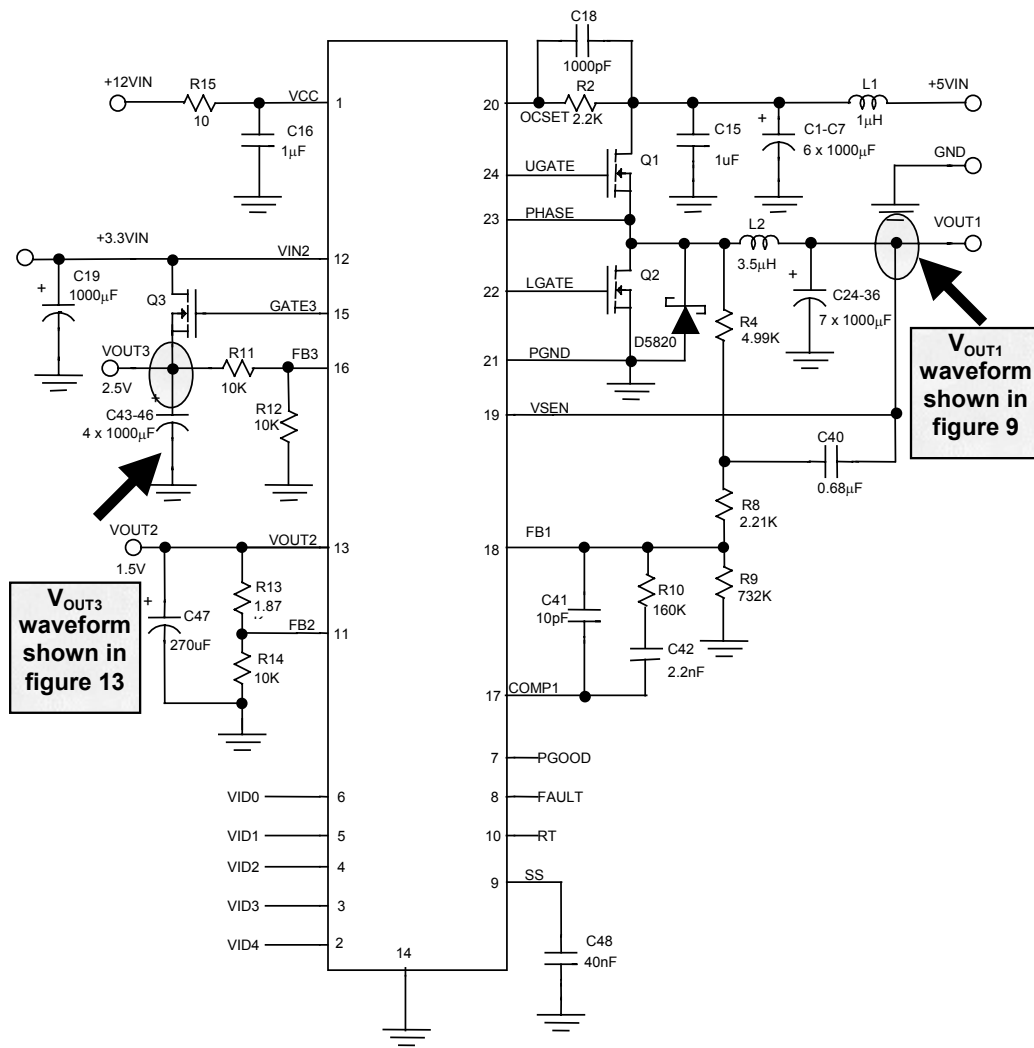


Figure 8. AIC1570 3 in 1 power solution for motherboard<sub>[3]</sub>

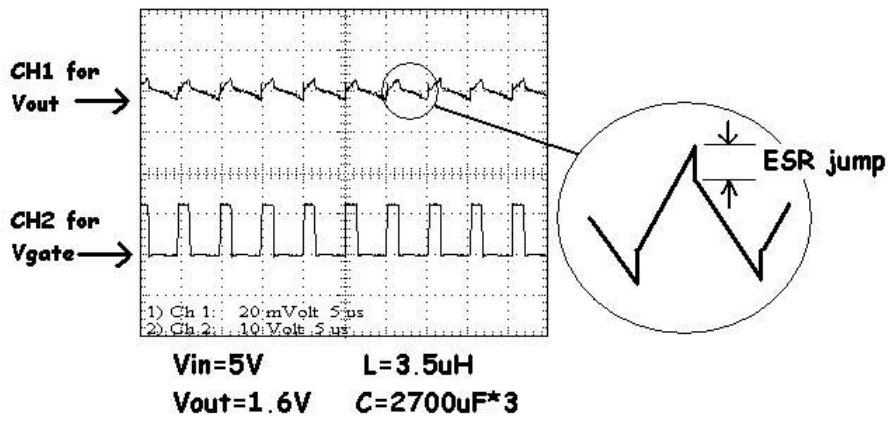


Figure 9.VOUT1 of AIC1570

Generally, we place several single capacitors in parallel, which reduce the total ESR. And figure 9 shows the real output voltage waveform when constant current pulled. It still dominates a certain percentage of the output variation although the effect of ESR jump is slight. Also, the waveform would be worse if neither the measurement is taken skillfully enough nor appropriately layout applied.

Figure 10 shows a 35A load current occurred in about 8A/us current slew rate. And figure 11 is a redraw waveform from figure 10, which presents clearer transient response.

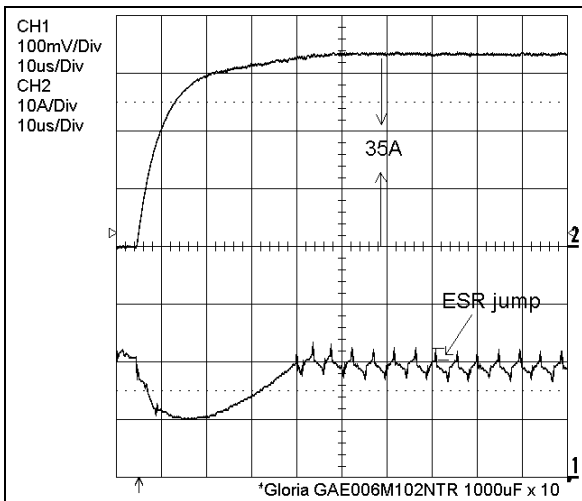


Figure 10.

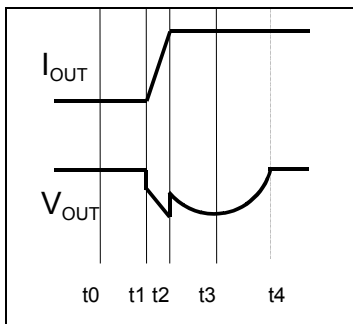


Figure 11.

The circuit is initiated at t=t0, during the rising or falling edge of the CPU supply current transient. A voltage drop is produced at t=t1 due to influence of ESR and ESL, which gives

$$V_{DROD@t1} = ESR \times \Delta I_{OUT} + ESL \frac{\Delta I_{OUT}}{\Delta t} \dots\dots(\text{equ.10})$$

After the initial transient, the ESL term in equation 10 drops off as in equation below

$$V_{DROD@t2} = ESR \times \Delta I_{OUT} \dots\dots\dots(\text{equ.11})$$

Within a clock cycle of the output current transient, the current feedback loop detects change of output current and increases power-switch duty cycle to maximum. Figure 12 shows the transient step and is followed by the description.

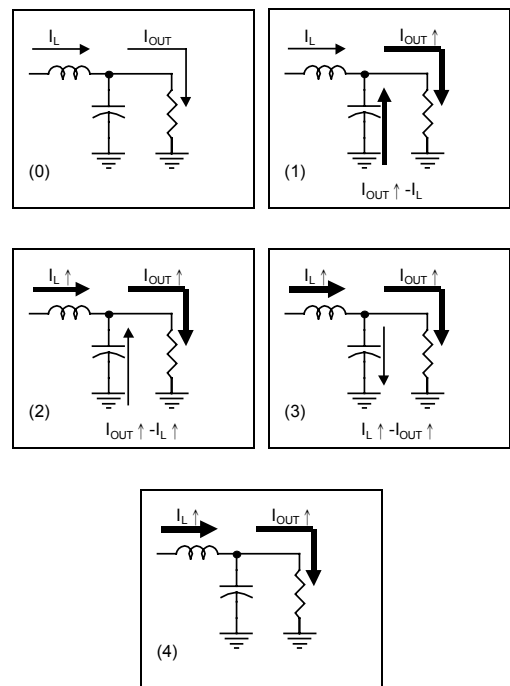


Figure 12. Transient current flow sequence

- (0) Circuit is initiated at  $t=t_0$
- (1) Capacitor provides most of transient current while output current transient occurs
- (2) The output inductor current starts to ramp up
- (3) Inductor current goes up to cover both of the output current and the current charge back to capacitor
- (4) Output current is provided by inductor current

**Linear output part**

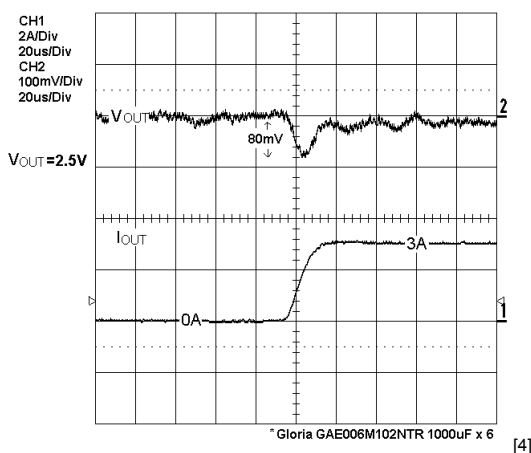
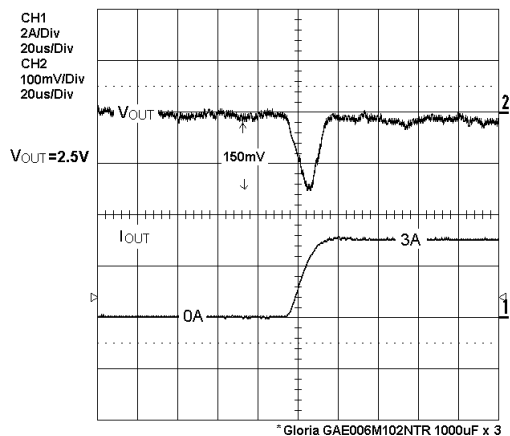


Figure 13. Output transient in LDO controller output

Figure 13 illustrates the output drop due to the unavoidable ESR and ESL effect, which follows the equation 11 and 12. And we can see the difference from the implementation of the larger and smaller output capacitors at the same test condition.

**Conclusion**

The following tips should be noticed to prevent your applications from ESR and ESL effects.

- Care must be taken for the different placement as shown in figure 14.
- An appropriate layout applied.
- Sufficient grounding implemented.
- Suitable measurement taken as in figure 15.

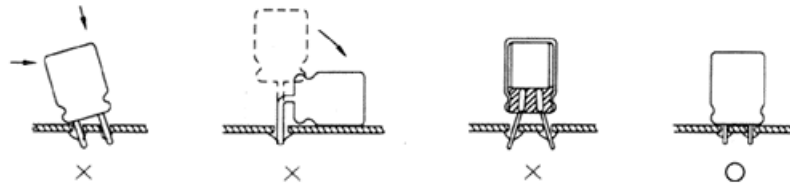


figure 14. The placement of capacitors<sup>[5]</sup>

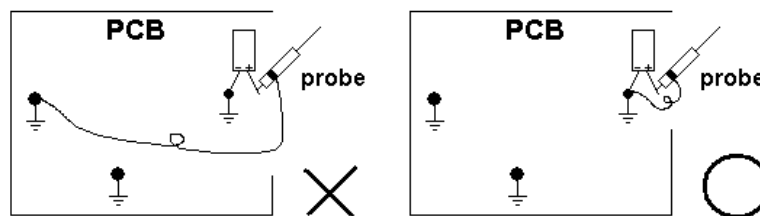


Figure 15. Correct measurement for transient response

**Reference**

[1] Harris Benson, University Physics, John Wiley & Sons, 1995, Chapter 26

[2] Philips T. Krein, Elements of Power Electronics, Oxford Univ Press, 1998, pp384-385, 392

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