

A Better Approach of Dealing with Ripple Noise of LDO

Hawk Chen

Introduction

It has been a trend that cellular phones, audio systems, cordless phones and portable appliances have a requirement for low noise power supplies. We are talking about an interesting subject how to control input noise caused by external disturbance and reduce output noise of LDO to provide power with lower noise for logic IC.

In general, the ripple noise of LDO power line will be influenced by a fast charge/discharge on capacitors out of the external switch converter and to LDO at input polarity, respectively. The power source of LDO is originally from the output of the converter. And the output is influenced by the ringing of current, which is caused by the rising and falling of edges of the switch MOSFET, on power line. It is a serious problem to generate noise and false signals at input polarity of LDO from power line. In order to avoid the problem, we employ some bypass capacitors or put the input capacitor as close as possible to the input polarity of LDO. In a high-speed environment, the inductive effect on power line and the input capacitor become very critical. The output polarity of high-speed switch generates high frequency noise on the power line. And the ringing makes LDO input capacitor with high lead inductor as an open circuit. The open circuit prevents the power line, flowing with current, from ripple noise on input polarity, high noises on output polarity and false signals on logic IC to maintain the system at a stable state. Conclusively, adding bypass capacitors (MLCC) or reducing inductor effect on

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The influence of inductor effect over LDO

- ◆ Formula of inductor effect on power line

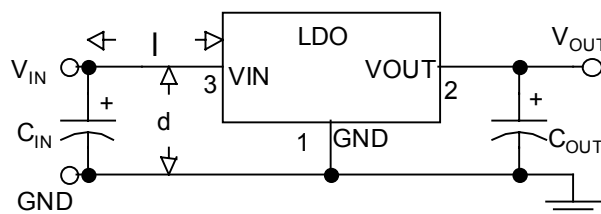


Figure 1: Inductor effect on power line

Most of the printed circuit boards are designed to maintain short distances from C_{IN} to the input polarity of IC as well as from power to ground. As a result, users may reduce the inductor effect on power line and lead inductor of capacitor. In addition, LDO has better reliable system due to a low-impedance path when bypass capacitor considered. As shown in figure1, the input capacitor is charged to prevent V_{IN} drop. Therefore, distance between C_{IN} and input polarity is a crucial point. The inductor will disturb power line when IC works normally. The inductor

effect is calculated as below:

$$L = l \frac{\mu_o}{\pi} \ln \frac{d}{r}$$

Where:

l: length of V_{IN} to input polarity of IC

d: distance of wires

r: radius of wire

μ_o : permeability of medium between wires

The inductor (L) is directly proportional to the distance between V_{IN} and input polarity of IC. In other words, the shorter the distances between V_{IN} and GND as well as V_{OUT} and GND, the less the inductor effect will be.

◆ Why is this location of input capacitor crucial to LDO?

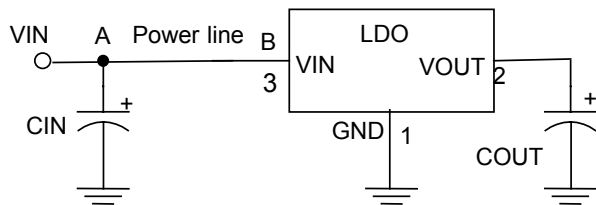


Figure 2: Power line distance between A and B

As shown in figure 2, the input polarity of LDO is disturbed due to the long distance from A to B. Printed circuit boards need to be designed with the shortest distance from C_{IN} to input polarity of IC as well as from power to ground.

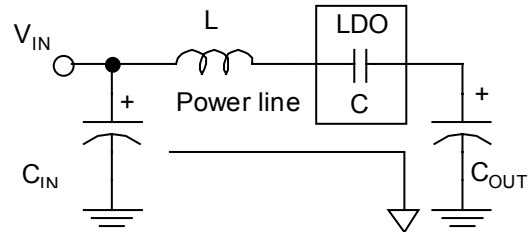


Figure 3: Power line equals inductor (L)

As shown in figure 3, LDO, a semiconductor component, is similar to the configuration of a capacitor because most of the semiconductor components possess charging and discharging functions. The inductor effect on the power line can be calculated as below:

$$L(\text{inductor}) = l \frac{\mu_o}{\pi} \ln \frac{d}{r} \text{ ----- (1)}$$

These series capacitors (C , C_{OUT}) can be calculated as:

$$\frac{1}{C_{IT}} = \frac{1}{C} + \frac{1}{C_{OUT}} \Rightarrow C_{IT} = \frac{C + C_{OUT}}{CC_{OUT}}$$

Thus, the ringing frequency (F) is shown as:

$$F = \frac{1}{2\pi\sqrt{LC_{IT}}} = \frac{1}{2\pi\sqrt{L \frac{C + C_{OUT}}{CC_{OUT}}}}$$

Where, ringing frequency (F) is an inverse proportional to C_{IT} . The reducing capacitance of C_{IT} will affect noise on input polarity of LDO and influence the stability of system.

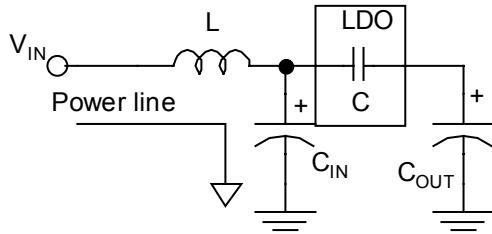


Figure 4: different location for input capacitor

Comparing figure 4 with figure 3, the input capacitor is located as close as possible to the input polarity, when the length of power line remains the same. Thus C_{IT} can be calculated as below:

$$C_{IT} = C_{IN} + \frac{C + C_{OUT}}{CC_{OUT}} \because C_{IN} \gg \frac{C + C_{OUT}}{CC_{OUT}} \approx C_{IN}$$

The ringing frequency (F) is shown as as:

$$F = \frac{1}{2\pi\sqrt{LC_{IT}}} = \frac{1}{2\pi\sqrt{LC_{IN}}}$$

As a result of the above, the ringing (F) will be reduced as the distance from input capacitor (C_{IT}) to the LDO input polarity becomes the shortest. Relocating the input capacitor can improve the ripple noise, however inductor effect on power line is still existing unless users implement the system with the shortest length of the power line, as required in formula (1).

Ripple rejection capability of LDO

◆ Measurement of PSRR

Power supply rejection ratio (PSRR), also known as ripple rejection, represents the performance of the LDO regulator, which prevents the regulated output voltage disturbance caused by input voltage variations. In particular, the PSRR filters out output

ripple noise when the switch mode power supply is used as the power of LDO in application.

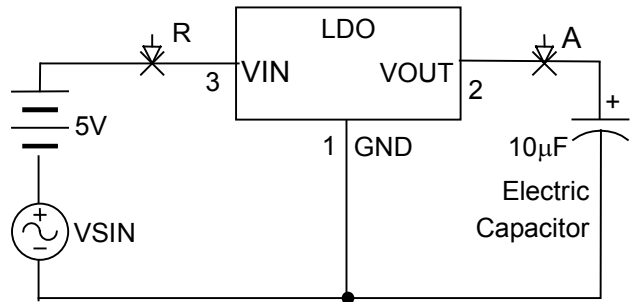


Figure 5: PSRR circuit of LDO measurement for HP3577A

Principle of PSRR calculation is defined by:

$$PSRR = \frac{A_{P-P}}{R_{P-P}} (dB)$$

Based on ripple rejection circuit, frequency from 0 to 300KHZ with amplitude 75mV, the PSRR of AIC1117-33 is shown as figure 6 below.

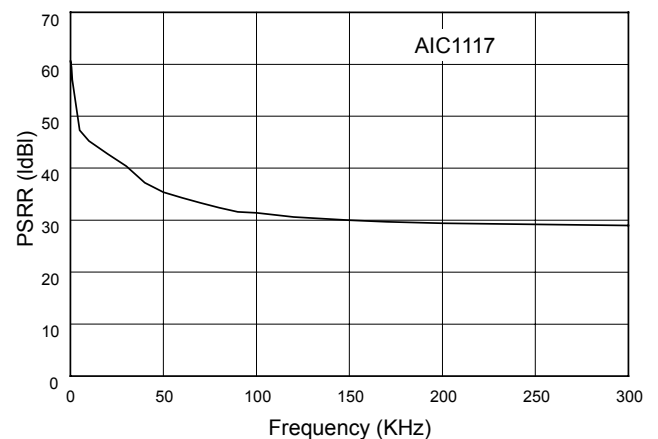


Figure 6: AIC1117 PSRR

◆ Simple measurement of PSRR

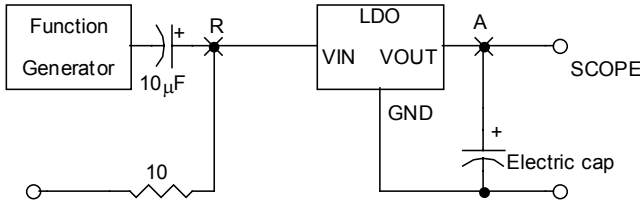


Figure 7: simple measurement circuit of PSRR

A sin AC waveform noise is at the negative pole of 10µF electric capacitor, which can separate AC signal from DC signal as in figure 7. And a bias 5V/DC, bearing a 60KHZ AC signal, is supplied to the input polarity of LDO, for example, AIC1117-33.

AIC1117-33 PSRR for 60KHZ can be calculated:

$$PSRR(dB) = 20 \log \left| \frac{A_{(p-p)}}{R_{(p-p)}} \right| dB = 20 \log \left| \frac{5.8mV}{155mV} \right| = 28.5dB$$

As shown in figure 8 and 9, the AIC1117-33 improves output ripple noise from 28.5dB to 34.9dB when the user employs 22µF electric capacitor, instead of 10µF, at input polarity.

Avoiding abnormal oscillation of LDO itself

◆ Properly selecting output capacitor

LDO, which features with output capacitor, does not produce any ripple noise itself, unless the input polarity is influenced by external ripple noise. For stability, an output (high ESR) capacitor is required between the LDO output and ground. Without this capacitor, the LDO will oscillate as temperature rising. Even though most of capacitors may work with the LDO, the equivalent series resistor (ESR) of the capacitors should be held within 5Ω. And capacitors of aluminum are recommended. In figure 10 and 11, the AIC1117-33 is applied with a load of 200mA current. Please refer to “guide to operate AIC1730 ceramic” for reasons of LDO oscillatory.

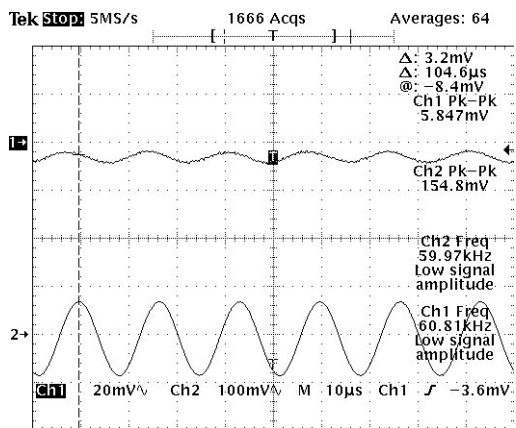


Figure 8: AIC1117-33 ripple rejection test

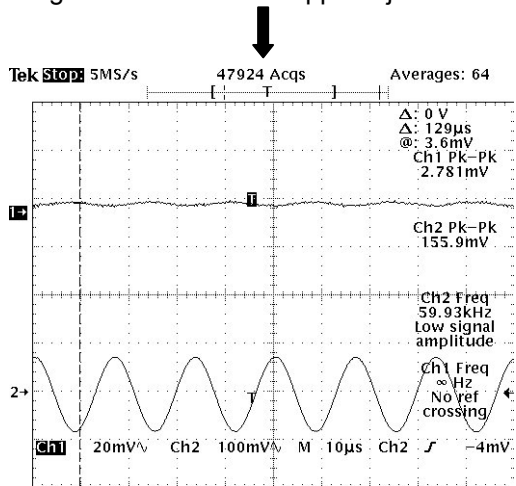


Figure 9: AIC1117-33 ripple rejection test

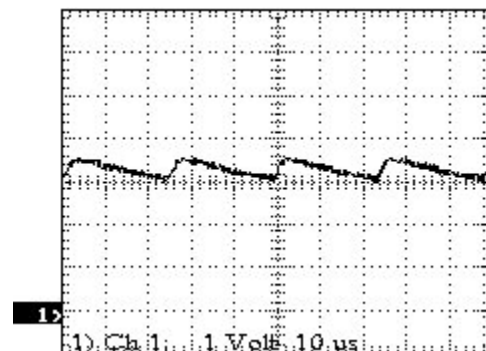


Figure 10: AIC1117-33 abnormal oscillation with an output of 10 μ F ceramic cap

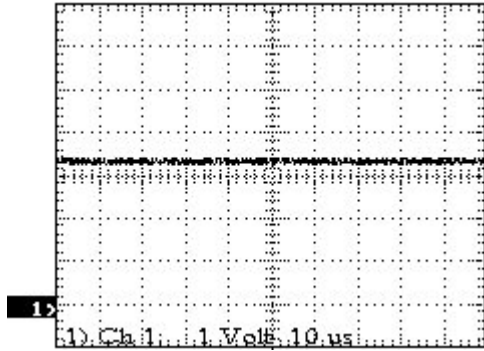


Figure 11: AIC1117-33 normal output voltage with an output of 10 μ F electric cap

◆ Properly selecting input capacitor

The employment of an input capacitor is necessary for LDO to avoid abnormal oscillation because the LDO does not have an external compensation pin. It is important to properly select input capacitor for most of the LDOs. When no input capacitor with a loading current on the output polarity applied, the zero point of the LDO loop-gain plot will be moving. And the movement of the zero point may cause the input polarity abnormally oscillated. Note that the input oscillation has influence on the output ripple noise. To avoid the noise caused by the oscillation, an input capacitor is an absolute requirement for the LDO. And a large input capacitance can definitely help the stability of the system. Shown as figure 12, the system is unstable state as no input capacitor on LDO. figure 13 shows satisfactorily dynamic impedance when input capacitor of LDO employed. With no input capacitor applied, abnormal oscillation occurs as in figure 14 and 15.

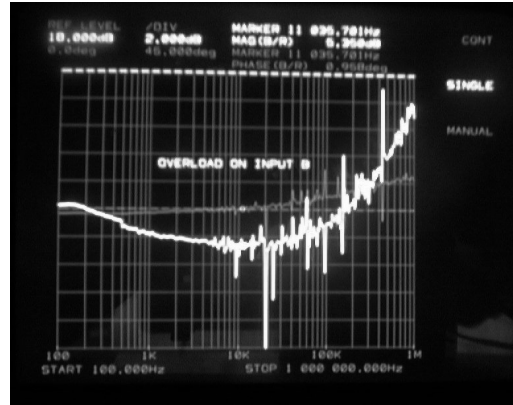


Figure 12: abnormal LDO dynamic impedance at loading 100mA

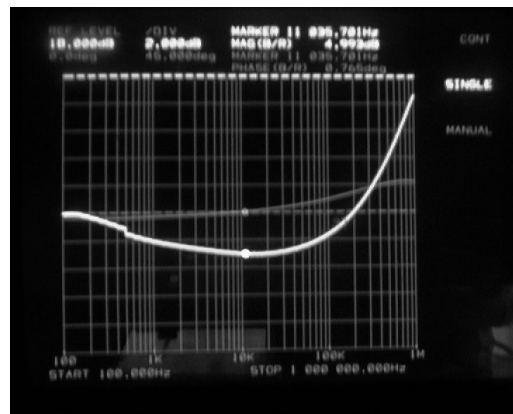


Figure 13: normal LDO dynamic impedance at loading 100mA

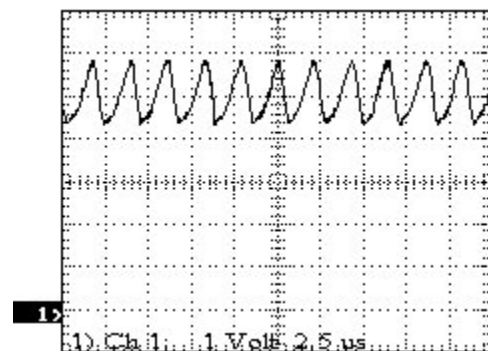


Figure 14: AIC1117-33 abnormal oscillation at input polarity

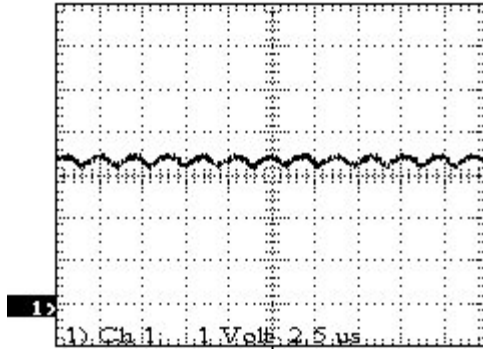


Figure 15: AIC1117-33 abnormal oscillation at output polarity

Conclusion

Conclusively, the major concern of the ripple noise is the power line length because the power line influences the system reliability indirectly through the inductor effect. Either locating the input capacitor as close as possible to the input polarity of LDO or adding some bypass capacitors on the power line may reduce the complications and completely eliminate the ringing. The concern of the power line

length on the PCB has always been left out of consideration when LDO is applied to a system.

Again, we would like to point out the importance of using the shortest power line to get the best LDO performance and reduce the disturbance from switching converter. It is always essential to minimize the loop among VIN, ground, input capacitor, and bypass capacitor.

Ripple rejection of LDO represents the capability of filtering noise. Users must be fully aware of the PSRR capability they need to select the proper ripple rejection capability of LDO.

Therefore, we are suggesting the users not only concern about the cost but also performance when they are making a decision on selecting an LDO.

Ripple noise has always been a complicated problem to some fields. And it is crucial to get the best resolution to solve abnormality and external disturbance. This can be obtained by a close attention to the layout and trace of PCB.

High ESR for output capacitor must be applied to LDO. Also employment of an input capacitor is highly recommended at the input polarity. They may result in the best and most efficient performance of the low dropout linear regulator.