A Handy Method to Obtain Satisfactory Response of Buck Converter

Hanns Chiu

Introduction

The focus of this application note is to help users to select a good set of components of the compensation section of the Buck converter. Traditionally, engineers first concern about the power circuit for a circuit design. After meeting the power requirement, what follows is control loop design. The first priority of control design is the stability. And after that, the choice of components can substantially effect the transient response. Here shows a simple method to obtain a satisfactory transient response with an acceptable steady state error.

1. Analysis:

Fig.1 shows the unity feedback system for Buck converter. We first identify transfer functions for each of the corresponding block.

As to the modeling of the low-frequency behavior of power switches in square-wave power converters, please refer to appendix [1]. The circuit of Buck converter is shown in Fig.2 and the model of its power switches is shown in Fig.3. Please note that the circuit in Fig.3 is linear. Fig.4 shows the circuit for small signal analysis.

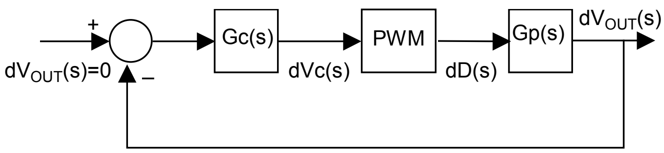

Fig.1 the unity feedback control loop for Buck converter

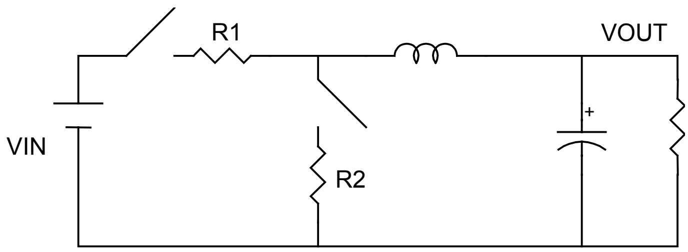

Fig. 2 Buck Converter

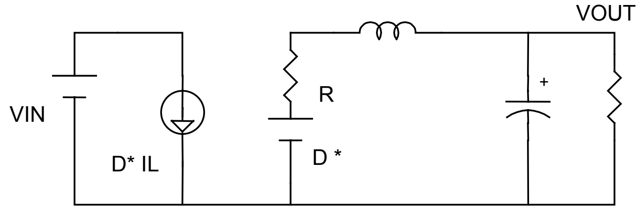

Fig.3 $R = DR_1 + (1 - D)R_2$

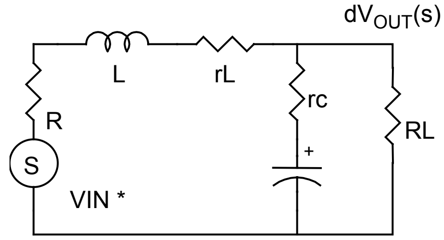

Fig. 4 Small Signal Circuit

The transfer function of output with respect to duty ratio is:

$$\frac{dV_{OUT}(s)}{dD(s)} = V_{IN} \times \frac{\dfrac{1}{\dfrac{1}{R_L} + \dfrac{1}{r_C + \dfrac{1}{sc}}}}{sL + (R + r_L) + \dfrac{1}{\dfrac{1}{R_L} + \dfrac{1}{r_C + \dfrac{1}{sc}}}}$$

……..(1)

$$= V_{IN} \times \frac{(CR_L r_C)s + R_L}{L(R_L C + r_C C)s^2 + [L + C(RR_L + r_L R_L + Rr_C + r_C r_L + R_L r_C)]s + (R_L + R + r_L)}$$

where:

V_{IN}: input voltage

V_{OUT}: output voltage

R: the equivalent resistance of power switches.

L: the inductor

C: the output capacitor

r_L: the DC resistance of inductor.

r_C: the ESR of output capacitor.

R_L: the loading of Buck converter.

when R_L is >> r_L , r_C and R

Equation 1 can be simplified as below:

$$\frac{dV_{OUT}(s)}{dD(s)} = V_{IN} \times \frac{r_C Cs + 1}{LCs^2 + [\dfrac{L}{R_L} + C(R + r_L + r_C)]s + 1}$$

$$= \frac{V_{IN} \times r_C}{L} \times \frac{s + \dfrac{1}{r_C C}}{s^2 + [\dfrac{1}{CR_L} + \dfrac{R + r_L + r_C}{L}]s + \dfrac{1}{LC}}$$

………………………………..(2)

where the zero Z_P is at $\frac{1}{r_C C}$

the $\omega_n = \frac{1}{\sqrt{LC}}$

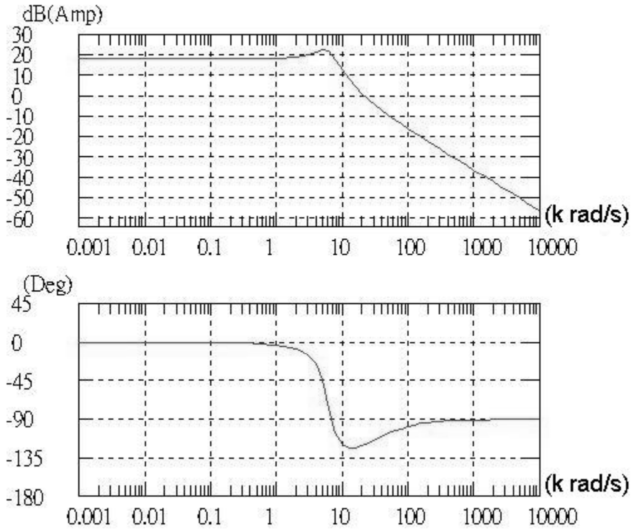

Fig. 5 The simulation of typical frequency response of Buck converter

Fig. 5 represents the simulation of typical frequency response of Buck converter. Note that the effect of complex conjugate poles of LC will make the gain curve at -40dB/decade and phase curve towards -180°. And after the region around ω_n, we will meet the zero, which is donated by the E.S.R of output capacitor. The gain curve becomes -20dB/decade and the phase is towards -90°.

As to the PWM (Pulse Width Modulation), its transfer function is

$$\frac{dD(s)}{dV_C(s)} = \frac{1}{V_M} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (3)$$

where V_M is the amplitude of ramp in PWM.

About the compensation network, we choose the type that is shown in Fig.5.

According to its frequency response in Fig.6, the network has high gain at low frequency, which helps to reduce the steady state error. The attenuation of gain at high frequency helps to weaken the noise disturbance.

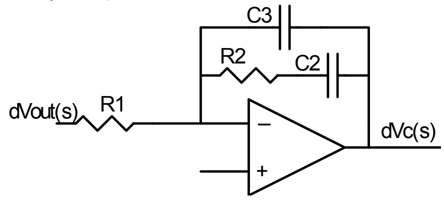

Fig.5 the compensation network

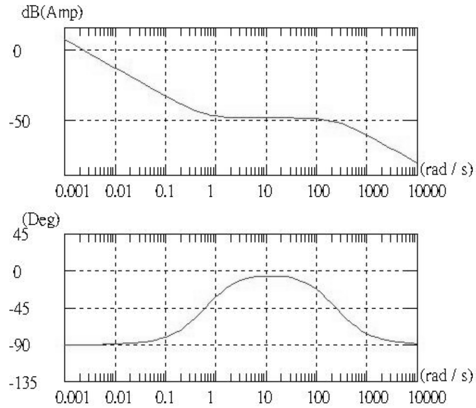

Fig.6 The simulation of typical frequency response of the compensation circuit

Its transfer function is:

$$\frac{dV_C(s)}{dV_{OUT}(s)} = \frac{1+R_2C_2s}{sR_1(C_2+C_3)[1+sR_2(C_2//C_3)]} \times \beta \ldots\ldots$$

$\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (4)$

Where:

the first pole P_0 is at zero frequency (ω=0).

one zero Z_1 is at $\frac{1}{R_2C_2}$

the 2nd pole P_2 is at

$$\frac{1}{R_2(C_2//C_3)} \approx \frac{1}{R_2C_3} \text{ (when C3<<C2)}$$

gain at low frequency: $G_C(s) = \frac{1}{sR_1(C_2+C_3)}$

gain at middle frequency:

$$G_C(s)=\frac{R_2C_2}{R_1(C_2+C_3)}\ \text{.....(Constant)}$$

gain at high frequency: $G_C(s)=\dfrac{1}{sR_1C_3}$

β is the gain of the feedback resistor divider. Note that due to the origin pole, the phase at low frequency is -90° and the gain curve is at -20dB/ decade. When the frequency approaches to zero, the phase increases toward 0° with a flat gain curve. When it moves toward the second pole, the frequency will be towards -90° and the gain curve goes back to -20dB/ decade again.

Control Strategy

The loop transfer function of Fig.1 is shown as below:

$$T(s)=G_C(s)\times PWM\times G_P(s)$$

$$=\frac{R_2C_2(s+\frac{1}{R_2C_2})}{sR_1(C_2+C_3)R_2(C_2//C_3)(s+\frac{1}{R_s(C_2//C_3)})}$$

$$\times\beta\times\frac{1}{V_M}\times V_{IN}\times\frac{r_C(s+\frac{1}{r_CC})}{L[s^2+(\frac{1}{CR_L}+\frac{R+r_C+r_L}{L})s+\frac{1}{LC}]}$$

..........(5)

After meeting the power circuit requirement, we start to design the control loop. Therefore the LC poles and output capacitor zero are already allocated. What we can do is to distribute the location of pole and zero of compensation network to achieve the desired response demand. To obtain high gain at low frequency, the origin pole is already set. Then here comes the strategy for the location of the zero and the second pole.

For the reason of stability, the zero of compensation network must be set lower than the zero of Buck converter. Without compensation zero, the zero of Buck converter would face three poles before it. The phase of the loop transfer function falls down toward -270° and passes through -180° between the poles of LC and the zero of Buck converter. This situation can lead to an unstable condition. To avoid that, the compensation circuit zero is advised to be lower than that of Buck converter. However the location of the compensation zero will affect the phase margin around the crossover frequency. To improve the phase margin of the loop transfer function and keep high gain at low frequency, the compensation zero is suggested between ω_n and $0.1\times\omega_n$. ($\omega_n=\dfrac{1}{\sqrt{LC}}$).

The second pole of compensation network is suggested far from the zero of Buck converter. In this way, we can obtain the –20dB/decade slope around the crossover frequency. According to the sampling theorem, the second pole of compensation network is suggested to be under one fifth of switching frequency of Buck converter ($\frac{1}{5}f_{Switching}$) to reduce the noise at high frequency.

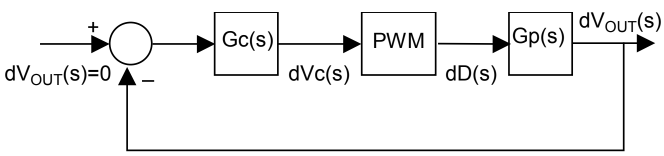

Fig.1 the unity feedback control loop for Buck converter

Design Example

Design example:

V_{IN}=8V,V_{OUT}=5V, the operation point of output current is 1A

L=27μH, r_L=38.5mΩ

C=1000μH, r_C=52mΩ

MOSFET=IR3103, R_{DS-ON}=14 mΩ

R_L=5Ω

V_M=1.3V

Design Procedure:

1. Construct the model of Buck converter and obtain the transfer function.

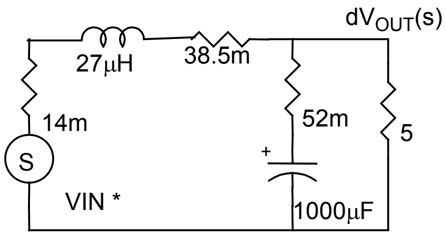

Fig.7 the model of the given Buck converter

$$\frac{dV_{OUT}(s)}{dD(s)} = 8 \times \frac{1.93k(s+19.2k)}{s^2+4.07ks+37M} \quad \text{…………….(6)}$$

From equation (6), the location of zero and the complex conjugate poles can be easily obtained.

2. Locate the zero and the second pole of compensation network.
   Since ω_n= 6.08k,
   zero of Buck= 19.2k,
   $f_{Switching}$= 200kHz= 1.25M(rad/s)
   Let zero of compensation network=2.04k
   Pole of compensation network=250k

3. Choose the components:
   According to the equation (4),
   Let R_2=75k then C_2=6800p, and C_3=56p

The transient response and the simulation of frequency response are shown in Fig. 8 and Fig. 9, respectively. Obviously, the rising time is too long and the overshoot is too large. To increase the speed of response and to have more phase margin, we try to extend the crossover frequency.

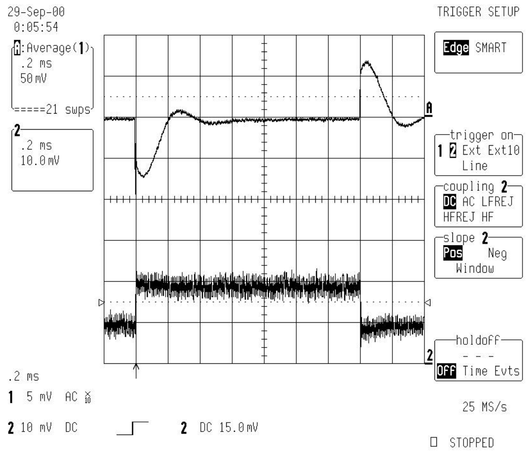

Fig.8 The transient response (Ch2 is current curve, 1A/div)

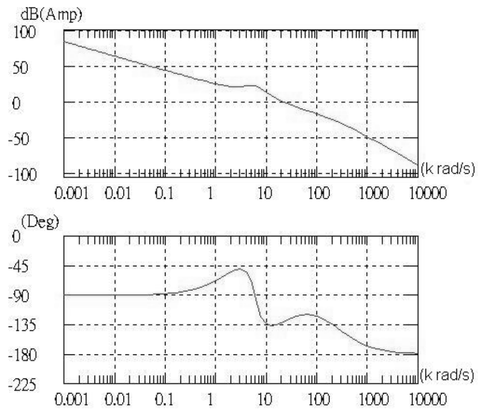

Fig. 9 The corresponding simulation of frequency response

2. According to equation (4), we can add the extra gain which is provided by the compensation network at the middle frequency without changing the location of zero and pole of the original loop transfer function.
   Let R_2=560k, then

$$R_2C_2=\frac{1}{2.04k} \qquad C_2=875\approx 820p$$

$$R_2C_3=\frac{1}{250k} \;\ldots\ldots\ldots\ldots\ldots\ldots\; C_3=7.14\approx 8p$$

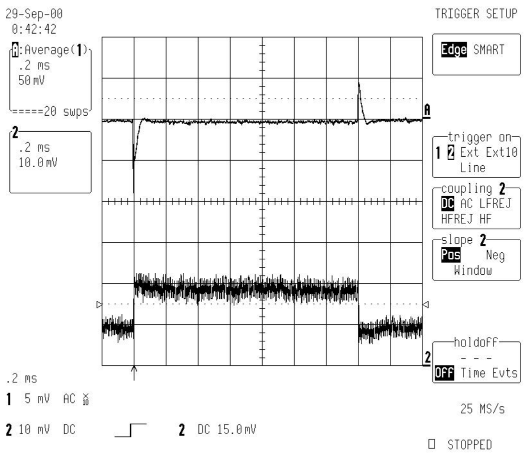

Fig.10 The transient response
(Ch2 is current curve, 1A/div)

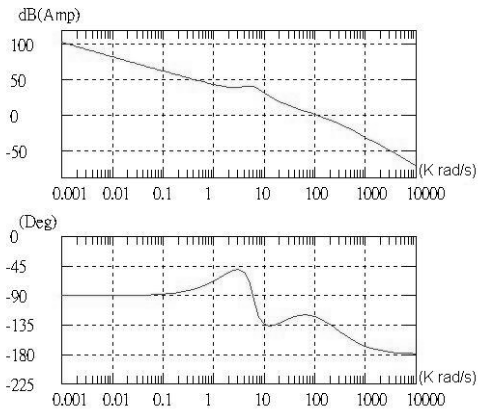

Fig.11 The corresponding simulation of frequency response

3. Referring to Fig. 11, the crossover frequency of open loop transfer function is raised. And we could also expect the bandwidth of the closed loop transfer function being increased. Indeed, in Fig 10, the set of control components, which we just used, shows high speed of response and less overshoot.

4. Although the pole at origin (according to equation (5)) means the infinitive gain at DC (ω=0), it is still a good idea to verify the steady state error by the load regulation. From Fig.12, it shows that the steady state error of two settings is small, and the two curves are almost identical.

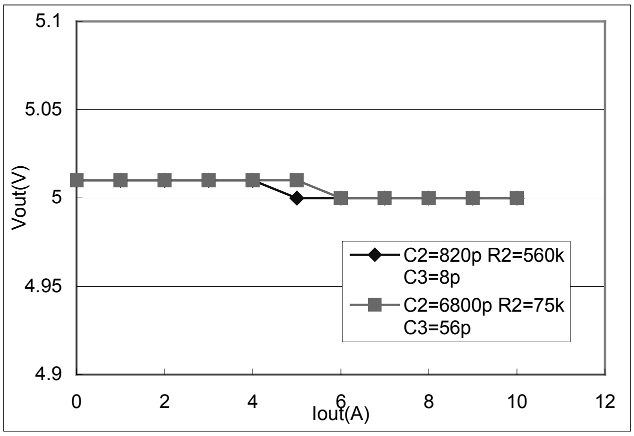

Fig.12 The comparison of load regulation of different components (V_{IN}=8V, V_{OUT}=5V)

5. From the results of transient response and the steady state error, the second set of components can achieve a satisfactory response.

5.Summary

By taking the advantage of a high gain at low frequency with a low gain at high frequency, the best performance of the Buck Converter can be achieved. The objectives are to improve the steady state error at low frequency and reduce noise disturbance at high frequency.

The key points of the compensation are:

1) Locate the zero around the LC resonant frequency for the issue of stability.

2) Locate the pole around $\frac{1}{5}f_{Switching}$ for the noise reduction at high frequency.

3) The combination of the above 2 procedures can

make the crossover frequency at the -20dB/ decade situation. Thus a satisfactory phase margin is achieved.

Reference:

[1] Yim-Shu Lee, Computer-Aided Analysis and Design of Switch-Mode Power Supplies., Marcel Dekker, Inc. Hong Kong,1993