

# Large Size Multilayer Ceramic Chip Capacitor (LCC Series)



## Features:

- Special internal design offers the highest voltage rating (50v to 8Kvdc)
- Capacitance range from 470 pF to 10 uF
- Sizes from 1515 to 7565
- Available with proprietary surface coating for arc prevention
- Available with flexible termination (Superterm) to minimize effects of mechanical stress
- 100% RoHS compliant
- Pd/Ag, 100% Sn and optional 90/10 Sn/Pb termination
- Available in NPO, X7R dielectrics
- Hi-Reliability testing is available

## Applications:

- Voltage Multipliers
- Power supplies
- DC-DC converters
- Surge protection
- Industrial control circuits
- Isolation
- Ballast
- Snubber
- Custom applications

## Summary of Specification:

### NPO Dielectrics:

Operating Temperature:	-55°C to 125°C	
Temperature Coefficient:	±30ppm/°C	
Capacitance Range:	100 pF – 470 nF	
Dissipation Factor (DF):	≤0.1%	
Insulation Resistance (IR):	100 GΩ or 1000 MΩ.uF whichever is less	
Aging:	0% per decade hr	
Dielectric Withstanding Voltage (DWV):	Rated Voltage (RV) ≤ 500V:	2.0x RV
	500 ≤ Rated Voltage (RV) < 1Kv	1.5x RV
	Rated Voltage (RV) ≥ 1000V	1.2x RV

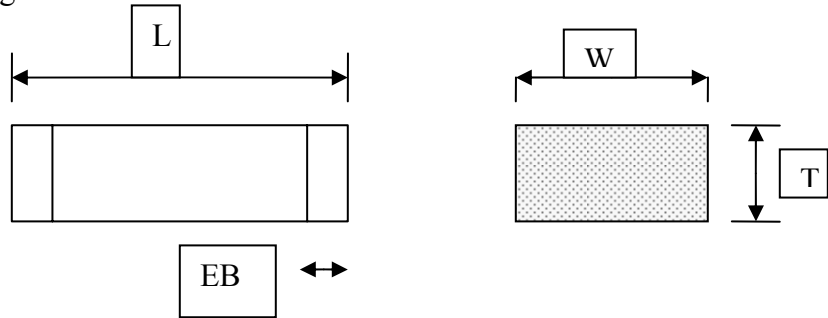
### X7R Dielectrics:

Operating Temperature:	-55°C to 125°C	
Temperature Coefficient:	±15%	
Capacitance Range:	820 pF - 10 uF	
Dissipation Factor (DF):	≤2.5%	
Insulation Resistance (IR):	100 GΩ or 1000 MΩ.uF whichever is less	
Aging:	2.5% per decade hr	
Dielectric Withstanding Voltage (DWV):	Rated Voltage (RV) ≤ 500V:	2.0x RV
	500 ≤ Rated Voltage (RV) < 1Kv	1.5x RV
	Rated Voltage (RV) ≥ 1000V	1.2x RV

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\*Maximum Capacitance and available voltages:



	L	W	T (Max)	EB	Dielectric	50V	100V	200V	500V	1KV	2KV	3KV	4KV	5KV	8KV
1515	0.15 (3.81)	0.15 (3.81)	0.15 (3.81)	.025 (0.64)	NPO	473	473	473	103	472	222	102			
					X7R	225	105	564	154	563	822	332			
1825	0.18 (4.57)	0.25 (6.35)	0.15 (3.81)	.025 (0.64)	NPO	104	104	104	473	153	562	272			
					X7R	825	475	225	474	124	223	103			
2220	0.22 (5.59)	0.20 (5.08)	0.15 (3.81)	.025 (0.64)	NPO	104	104	683	473	153	562	272	122	471	
					X7R	825	475	225	474	124	223	103	222	102	
2225	0.22 (5.59)	0.25 (6.35)	0.15 (3.81)	.025 (0.64)	NPO	124	124	124	563	183	822	332	152	681	
					X7R	106	475	275	684	184	473	153	472	222	
2520	0.25 (6.35)	0.20 (5.08)	0.15 (3.81)	.025 (0.64)	NPO	104	104	104	473	153	562	272	102	471	
					X7R	825	475	225	474	124	223	103	222	152	
3530	0.35 (8.89)	0.30 (7.62)	0.20 (5.08)	.025 (0.64)	NPO				823	473	153	682	332	102	471
					X7R				105	224	473	153	562	222	821
3640	0.36 (9.14)	0.40 (10.16)	0.20 (5.08)	.025 (0.64)	NPO				823	473	153	682	332	102	471
					X7R				105	274	473	183	682	222	821
4540	0.45 (11.43)	0.40 (10.16)	0.20 (5.08)	.025 (0.64)	NPO				124	563	223	123	682	272	821
					X7R				185	474	104	473	273	223	222
5550	0.55 (13.97)	0.50 (12.7)	0.20 (5.08)	.025 (0.64)	NPO				224	823	333	183	103	332	122
					X7R				225	684	184	823	333	273	272
6560	0.65 (16.51)	0.60 (15.24)	0.20 (5.08)	.025 (0.64)	NPO				334	104	473	223	153	472	222
					X7R				335	824	224	104	473	333	472
7565	0.75 (19.05)	0.60 (16.51)	0.20 (5.08)	.025 (0.64)	NPO				474	224	563	473	223	562	332
					X7R				475	105	334	224	683	473	682

- All dimensions are in Inches (mm)
- All dimension tolerances are  $\pm 0.020''$  ( $\pm 0.51$  mm)

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\*How to order:

C	3530	X	105	K	501	T	X	O	
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Product Code	Chip Size	Dielectrics	Capacitance	Tolerance	Rated Voltage	Packaging	Termination	Special Requirement	Testing requirement
C: MLCC	Ex: 3530:0.35"X0.30"	N: NPO X: X7R	Two significant digit + number of zero (in pF) Ex: 105: 1000000pF =1uF	F: ±1% G: ±2% J: ±5% K: ±10% M: ±20%	050: 50v 101: 100v 201: 200v ..... 502: 5Kv 802: 8Kv	B: Bulk T: Tape and Reel	S: Solderable Ag P: Pd/Ag N: 100% Sn plated X: superterm W: 90Sn/10Pb	Blank: No coating O: Arc prevention coating M: Marked A: Marked+Arc prevention Coating	Blank: Standard electrical test H: Hi-Rel

\*Soldering and Handling Precautions:

Due to geometry and mass, large ceramic capacitors have an increased susceptibility to thermal and mechanical cracking. To minimize the likelihood of cracking, capacitors should be handled carefully and stored in the waffle pack containers, carrier tape or other suitable containers until use. Care should be taken that capacitors do not come in contact with each other causing ceramic chip-outs.

The recommended method for soldering large chips, is reflow soldering. Wave soldering and manual soldering with an Iron is not recommended. Ceramic capacitors must be preheated and cooled at a rate less than 3°C/sec to within 50°C of the peak reflow temperature. Sudden increases, or decreases in temperature beyond the recommended rate, may cause thermal cracks.

\* Available Options:

- HEC offers polymer termination (superterm) for very large chips to minimize mechanical cracks due to board flexing.
- To minimize the potential for surface arcing in higher voltage applications, HEC offers the option of a proprietary surface coating.
- Pure Tin terminated/ROHS compliant products are offered as a standard, however, lead (Pb) content plated termination may be provided if required.
- Pd/Ag termination is also offered as an option for Hybrid circuits and other applications.